EXHIBIT 8

MPS Accused Products

The following list of Accused Products is exemplary, non-exhaustive, and non-limiting. Greenthread identifies the following specific products to illustrate categories or types of products that constitute a MPS Accused Products. Greenthread further asserts claims against all product variations and part numbers of the MPS Accused Products. All of the below exemplar product categories were identified by MPS at https://www.monolithicpower.com/en/products.html

	MPS Accused Product Categories/Types
1.	Switching converters and controllers
2.	Multi-phase controllers
3.	Power management integrated circuits
4.	USB switches
5.	Load switches
6.	MOFSET drivers
7.	Isolated gate drivers
8.	Digital isolators
9.	Isolated DC/DC converters
10.	Power modules
11.	Battery chargers and monitors
12.	Fuel gauges
13.	Stepper motor drivers
14.	Brushless DC pre-drivers
15.	Brushless DC motor controllers
16.	Brushed DC drivers
17.	Fan drivers
18.	Backlight drivers
19.	Audio drivers
20.	Analog-to-digital converters
21.	Angular position sensors
22.	Current sensors

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

U.S. Patent No. 10,510,842	Accused Products MPS Semiconductor 86905 SiC N-Channel MOSFET
[Claim 1, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the MPS Accused Products include a semiconductor device. This chart includes exemplary information regarding a representative example of the MPS Accused Products, the MPS Semiconductor 86905 Intelli-Phase Solution with integrated HS/LS-FETs and Driver ("86905"). The 86905 was analyzed in the below referenced report from Tech Insights. MPS MP86905 Intelli-PhaseTM Solution with Integrated HS/LS-FETs and Driver Power Essentials Summary ("MP86905 Report"), *available at* https://library.techinsights.com/search/device-details?tab=reports&id=PEF-2202-801&genealogyCode=MPS-MP9502. The 86905 was also analyzed in a supplemental report from Tech Insights ("MP86905 Supplemental Report"). *See* Exhibit 8 (Supplemental Report for PEF-2202-801). The complete reports are hereby incorporated by reference into each and every claim and claim element discussed. Selected pages are reproduced herein to aid in understanding. The MPS 86905 is representative of the MPS Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other MPS Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '842 patent (and the other asserted patents). For example, the other MPS Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '842 patent (and the other asserted patents). The claimed invention would have application in numerous types of MPS products, including switching converters and controllers, multi-phase controllers, power management integrated circuits, USB switches, load switches, MOFSET drivers, insolated gate drivers, digital isolators, isolated DC/DC converters, power modules, battery chargers and monitors, fuel gauges, stepper motor drivers, brushless DC pre-drivers, brushless DC motor controllers, brushed DC drivers, fan drivers, backlight drivers, audio drivers, analog-to-digital converters, angular position sensors, and current sensors, because such products would benefit from, among other things, improved switching time for transistors in the device. Therefore, upon information and belief the other MPS Accused Products contain similar features as the MPS 86905 transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other MPS Accused Products contain similar features as the MPS 86905, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery. The MPS Accused Products, of which MPS 86905 is one example, are semiconductor devices.

Device Summary

- This report presents a Power Essentials analysis of the MPS MP86905 silicon (Si)-based power management IC (PMIC). The MP86905 is a monolithic half-bridge with built-in internal power MOSFETs and gate drivers and is ideally suited for multi-phase buck regulators. It offers 50 A continuous output current over a wide 4.5 V to 16 V operating input range [2].
- The MP86905 comprises a single die with MP9502 die markings, which are encapsulated in a 23-pin flip-chip quad-flat-no-lead (FC-QFN) package with likely copper (Cu) bumping directly to the leadframe.
- The MP9502 die substrate is ~155 µm thick including the upper epitaxy layer and uses Bipolar-CMOS-DMOS (BCD) technology. It features a single layer of polysilicon in the analyzed regions, three aluminum (Al) metal layers, tungsten (W) contacts and vias, cobalt silicide (CoSi) at the source, drain, and polysilicon contact regions. The pre-metal dielectric (PMD) uses silicon oxide (SiO) layers, while the inter-metal dielectric (IMD) layers uses oxide as well. Isolation structures include shallow trench isolation (STI) in the logic region.
- One group of high side MOSFET (HSFET) array and two groups of low side MOSFET (LSFET) array are used on the die. The structure and dopants of the HS/LS FET arrays are analyzed. Dopant analysis in the HS/LS FET array region shows the use of a P-type substrate, an N-type buried layer (NBL), a N-drift/N-well layer and a P-well layer.
- The stepped-gate-oxide (SGO) is used in the LDMOS devices on this die. The use of SGO allows a reduction of on-resistance (Ron) compared with the conventional STI LDMOS [3].
- The HSFET is arranged in a one-dimensional (1D) array with a ~4.0 µm drain-to-drain pitch and ~0.66 µm total polysilicon gate length, while the LSFET is arranged with ~3.4 µm drain-to-drain pitch and ~0.60 µm total polysilicon gate length in total.
- In the logic region, the minimum observed gate length is 0.40 µm on a 0.86 µm contacted gate pitch, indicating the use of likely 0.18 µm process generation with relaxed feature dimensions.

Manufacturer	Monolithic Power Systems
Part number	MP86905
Foundry	Unknown
Type	PMIC
Date code	H39 (week 39 of 2017)
Package type	23-pin FC-QFN
Package markings	MPSH39 M86905 54U403
Package dimensions	3.97 mm × 3.97 mm × 0.88 mm (thick)
Die markings	MP9502 2013 <MPS logo>
Die size (whole die)	3.38 mm × 3.14 mm (10.61 mm²)
Die size (edge seal)	3.36 mm × 3.12 mm (10.48 mm²)
Minimum measured transistor gate length/pitch	0.40 µm/0.86 µm
Process generation	Likely 0.18 µm process generation with relaxed feature dimensions
Feature measured to determine process generation	Contacted gate pitch, use of CoSi contacts, STI isolation
Maximum voltage [2]	18 V

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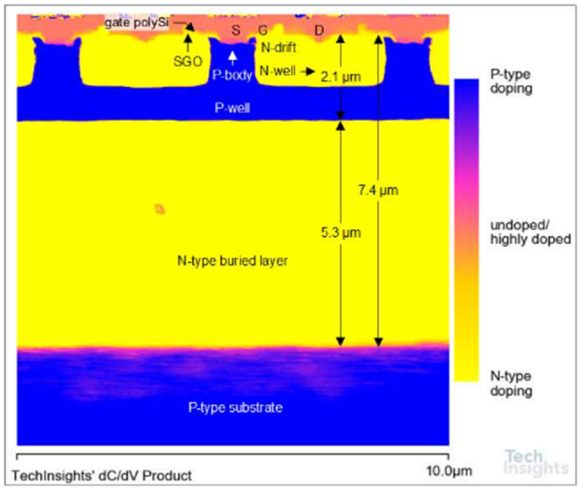
MP86905 Report at 5.

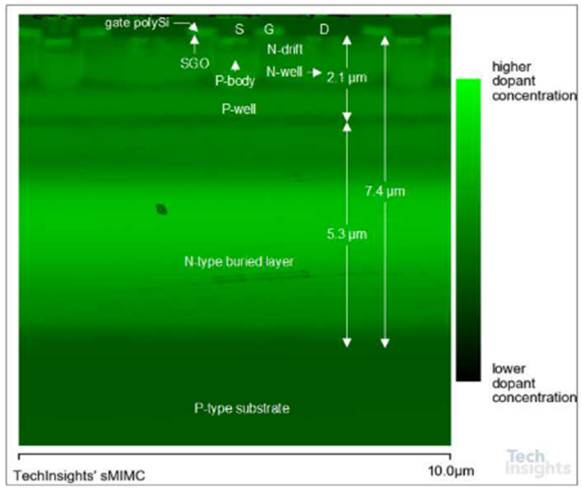
MP9502 Die HSFET Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the HSFET array show the use of a P-type body region, N-type drift region, and a higher-doped N-well at the drain region.
- The P-well layer starts ~2.1 µm from the front surface, while the NBL measures ~5.3 µm thick and reaches ~7.4 µm deep.
- NBL seems to have two regions of higher-doped lower portion and lower-doped upper portion in the Si body.



Array_040522164608_PRODUCT_FRW_10.0u_512p_400973.png

HSFET Array – SCM Cross-Section A-A



Array_040522164608_SMIMC_FRW_10.0u_512p_400973.png

HSFET Array – sMIM-C Cross-Section A-A

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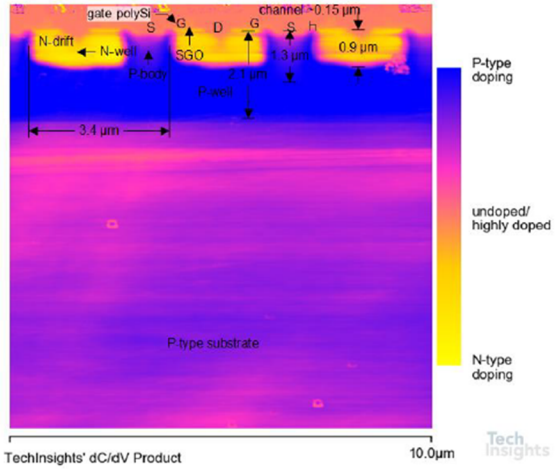
MP86905 Report at 42.

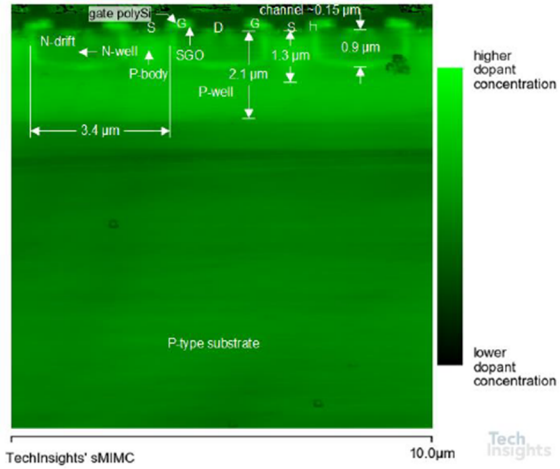
MP9502 Die LSFET Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the LSFET array show the use of a P-type body region, shallower N-drift/N-well in the drain region, and NBL is absent in the LSFET array.
- The P-well is ~2.1 µm deep, the P-body is ~1.3 µm deep, while the drain N-drift/N-well is ~0.9 µm deep, shallower than 1.2 µm observed in the HSFET array.
- Both HSFET and LSFET array likely share the P-well and P-body masks, but use different mask for drain drift region.
- The effective channel length defined by dopant boundary is estimated to be ~0.15 µm in the LSFET array.



Array_2_040622155352_PRODUCT_FRW_10.0u_512p_400973.png

LSFET Array – SCM Cross-Section A-A



Array_2_040622155352_SMIMC_FRW_10.0u_512p_400973.png

LSFET Array – sMIM-C Cross-Section A-A

2

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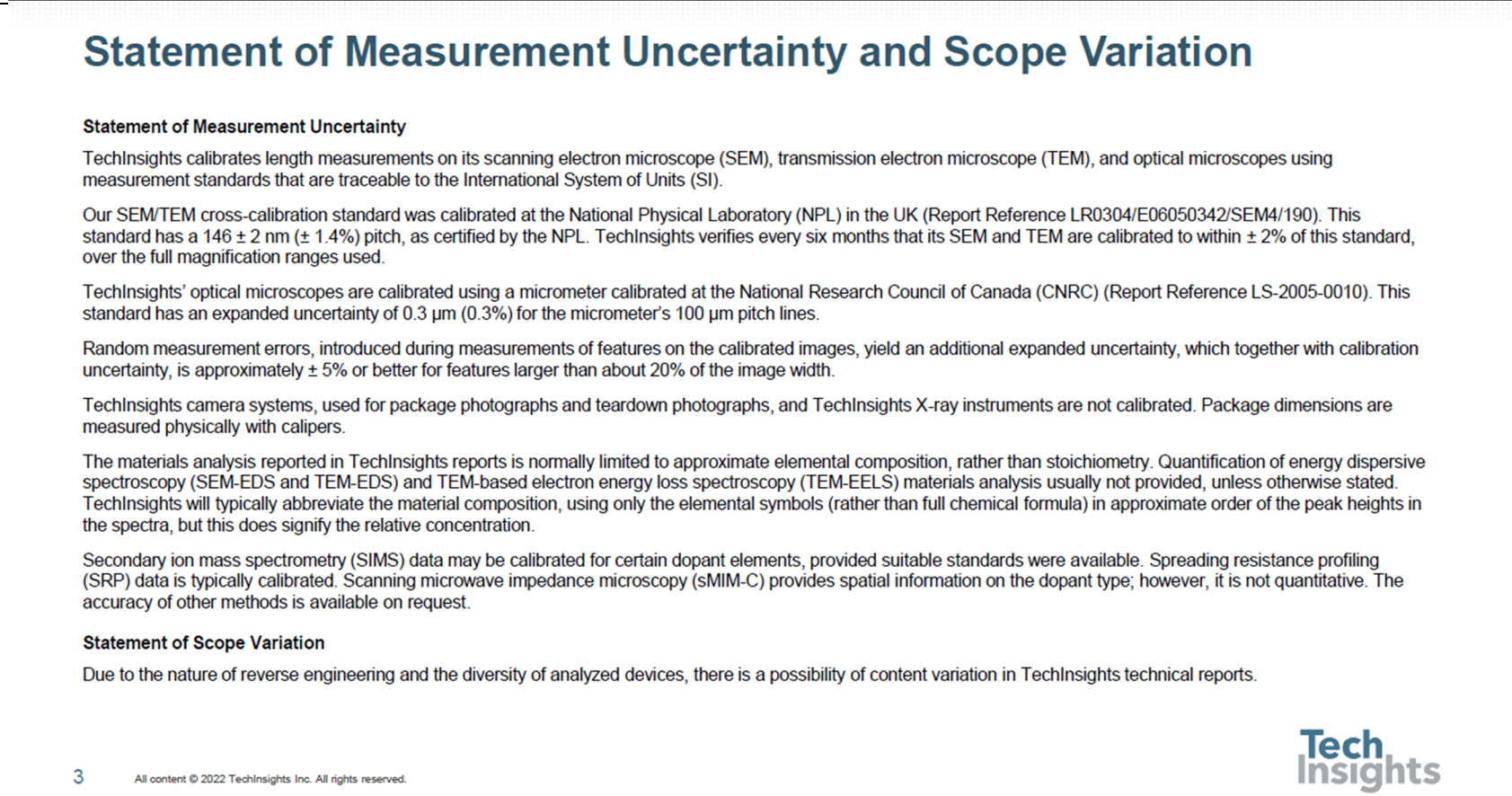
MP86905 Supplemental Report at 2.



Statement of Measurement Uncertainty and Scope Variation

Statement of Measurement Uncertainty

TechInsights calibrates length measurements on its scanning electron microscope (SEM), transmission electron microscope (TEM), and optical microscopes using measurement standards that are traceable to the International System of Units (SI).

Our SEM/TEM cross-calibration standard was calibrated at the National Physical Laboratory (NPL) in the UK (Report Reference LR0304/E06050342/SEM4/190). This standard has a 146 ± 2 nm (± 1.4%) pitch, as certified by the NPL. TechInsights verifies every six months that its SEM and TEM are calibrated to within ± 2% of this standard, over the full magnification ranges used.

TechInsights' optical microscopes are calibrated using a micrometer calibrated at the National Research Council of Canada (CNRC) (Report Reference LS-2005-0010). This standard has an expanded uncertainty of 0.3 µm (0.3%) for the micrometer's 100 µm pitch lines.

Random measurement errors, introduced during measurements of features on the calibrated images, yield an additional expanded uncertainty, which together with calibration uncertainty, is approximately ± 5% or better for features larger than about 20% of the image width.

TechInsights camera systems, used for package photographs and teardown photographs, and TechInsights X-ray instruments are not calibrated. Package dimensions are measured physically with calipers.

The materials analysis reported in TechInsights reports is normally limited to approximate elemental composition, rather than stoichiometry. Quantification of energy dispersive spectroscopy (SEM-EDS and TEM-EDS) and TEM-based electron energy loss spectroscopy (TEM-EELS) materials analysis usually not provided, unless otherwise stated. TechInsights will typically abbreviate the material composition, using only the elemental symbols (rather than full chemical formula) in approximate order of the peak heights in the spectra, but this does signify the relative concentration.

Secondary ion mass spectrometry (SIMS) data may be calibrated for certain dopant elements, provided suitable standards were available. Spreading resistance profiling (SRP) data is typically calibrated. Scanning microwave impedance microscopy (sMIM-C) provides spatial information on the dopant type; however, it is not quantitative. The accuracy of other methods is available on request.

Statement of Scope Variation

Due to the nature of reverse engineering and the diversity of analyzed devices, there is a possibility of content variation in TechInsights technical reports.

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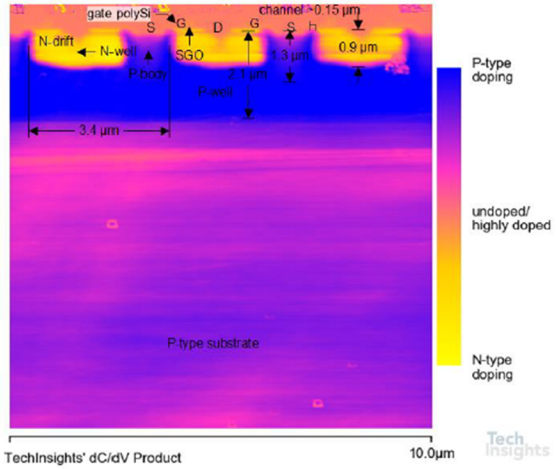
MP86905 Supplemental Report at 3.

[Claim 1, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The MPS Accused Products include/comprise a semiconductor device comprising a substrate of a first doping type at a first doping level having first and second surfaces. For example, analysis of an exemplary MPS Accused Product (the MPS 86905 discussed above) reveals the presence of such a substrate. For example, the MPS 86905 discussed above for Claim 1, Preamble, was imaged using scanning electron microscopy (SEM) scanning capacitance/microwave impedance microscopy (SCM/SMIM) analysis.

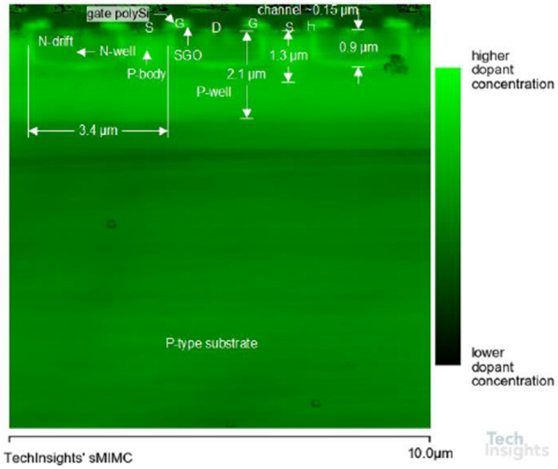
MP9502 Die LSFET Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the LSFET array show the use of a P-type body region, shallower N-drift/N-well in the drain region, and NBL is absent in the LSFET array.
- The P-well is ~2.1 µm deep, the P-body is ~1.3 µm deep, while the drain N-drift/N-well is ~0.9 µm deep, shallower than 1.2 µm observed in the HSFET array.
- Both HSFET and LSFET array likely share the P-well and P-body masks, but use different mask for drain drift region.
- The effective channel length defined by dopant boundary is estimated to be ~0.15 µm in the LSFET array.



Array_2_040622155352_PRODUCT_FRW_10.0u_512p_400973.png

LSFET Array – SCM Cross-Section A-A



Array_2_040622155352_SMIMC_FRW_10.0u_512p_400973.png

LSFET Array – sMIM-C Cross-Section A-A

2

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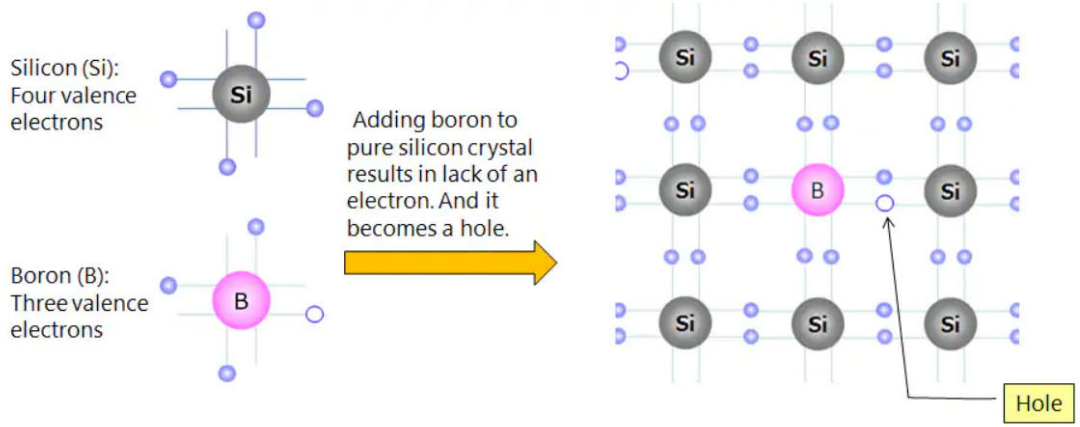
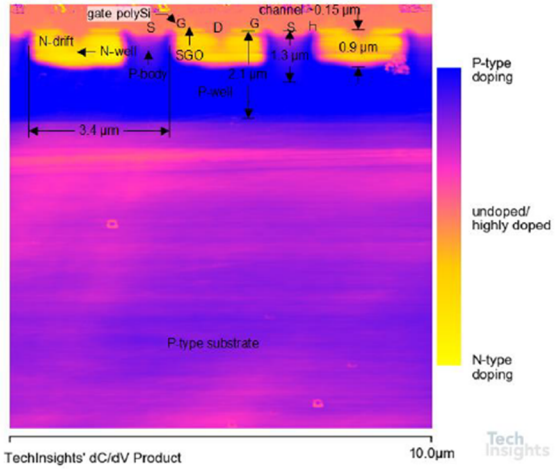
MP86905 Supplemental Report at 2.

	What is a p-type Semiconductor? A p-type semiconductor is an intrinsic semiconductor doped with boron (B) or indium (In). Silicon of Group IV has four valence electrons and boron of Group III has three valence electrons. If a small amount of boron is doped to a single crystal of silicon, valence electrons will be insufficient at one position to bond silicon and boron, resulting in holes* that lack electrons. When a voltage is applied in this state, the neighboring electrons move to the hole, so that the place where an electron is present becomes a new hole, and the holes appear to move to the "–" electrode in sequence.  * This hole is the carrier of a p-type semiconductor. *See* https://toshiba.semicon-storage.com/us/semiconductor/knowledge/e-learning/discrete/chap1/chap1-4.html#:~:text=A%20p%2Dtype%20semiconductor%20is,III%20has%20three%20valence%20electrons.
[Claim 1, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which	The MPS Accused Products, and products incorporating them, include/comprise a semiconductor device comprising a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed. For example, as shown in imagery from the Tech Insights Report, the exemplary MPS 86905 scanning capacitance/microwave impedance microscopy (SCM/SMIM) analysis includes a first active region disposed adjacent the first surface of the substrate. *See* below showing "HSFET Array," and toward the top the source ("S"), gate ("g") and drain ("drain") where the transistors are, underneath each of the annotations are active regions. *See also* below showing "LSFET Array."

transistors can be formed;

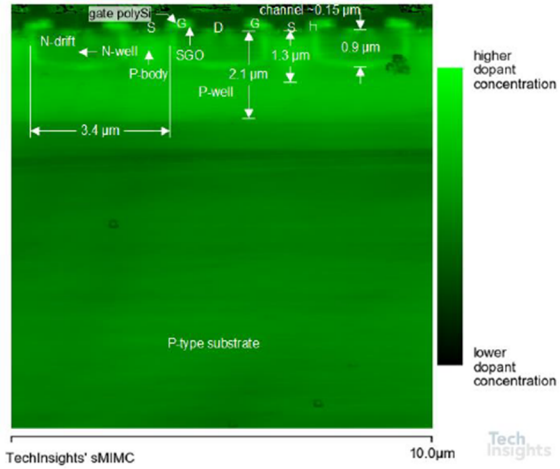
MP9502 Die LSFET Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the LSFET array show the use of a P-type body region, shallower N-drift/N-well in the drain region, and NBL is absent in the LSFET array.
- The P-well is ~2.1 µm deep, the P-body is ~1.3 µm deep, while the drain N-drift/N-well is ~0.9 µm deep, shallower than 1.2 µm observed in the HSFET array.
- Both HSFET and LSFET array likely share the P-well and P-body masks, but use different mask for drain drift region.
- The effective channel length defined by dopant boundary is estimated to be ~0.15 µm in the LSFET array.



Array_2_040622155352_PRODUCT_FRW_10.0u_512p_400973.png

LSFET Array – SCM Cross-Section A-A



Array_2_040622155352_SMIMC_FRW_10.0u_512p_400973.png

LSFET Array – sMIM-C Cross-Section A-A

2

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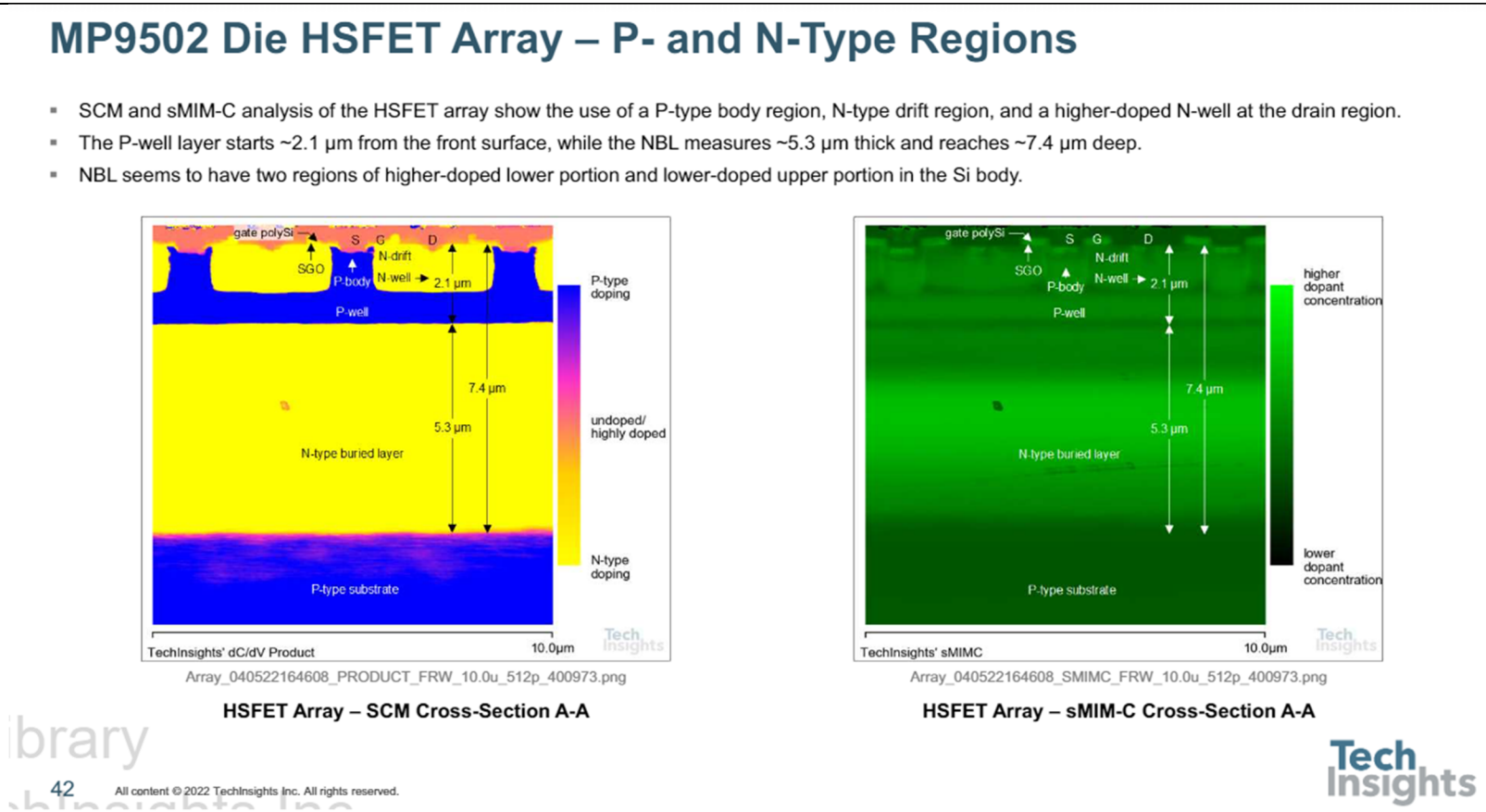
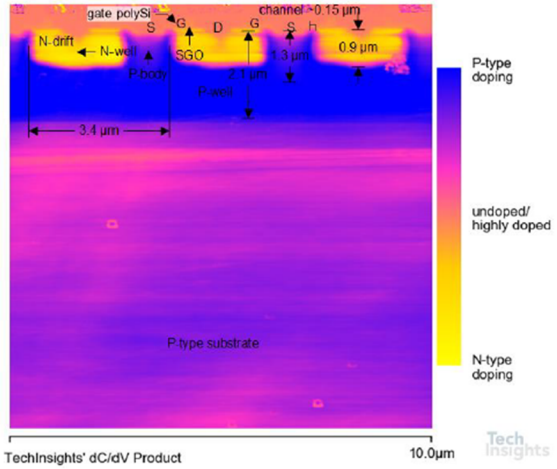
MP86905 Supplemental Report at 2.

	 MP86905 Report at 42.
[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and	The MPS Accused Products include a semiconductor device comprising a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed. For example, the HSFET and LSFET arrays shown in the images reproduced at Claim 1, Element 2 shows multiple transistors with active regions.

within which transistors can be formed;	
[Claim 1, Element 4] transistors formed in at least one of the first active region or second active region; and	The MPS Accused Products include a semiconductor device comprising transistors formed in at least one of the first active region or second active region. *See* above at Preamble, Elements 2-3 (discussing the HSFET AND LSFET arrays).
[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate.	The MPS Accused Products meet this limitation. *See* above at Element 1. For example, this is shown by the scanning capacitance/microwave impedance microscopy (SCM/sMIM) analysis. SCM/sMIM electrically characterizes the tested device and generates maps, which provide graphical representation of the dopant types and concentrations by measuring carrier movement as they are attracted to or repulsed by the probe. The SCM/SMIM maps taken from MPS Accused Products shown herein demonstrate differences in carrier concentration as a function of depth, which generate electric fields within the accused products. The contrast in the SMIM image is proportional to the capacitance of the sample under inspection, so that brighter green corresponds to higher dopant concentration, and darker green/black corresponds to lower dopant concentration. Likewise, the SCM images above show doping concentration and doping type as indicated in the legends to the right. Zooming in on the sMIM-C image taken from page 43 of the Tech Insights report clearly shows vertical dopant grading in the active regions surounding the source, gate, and drain. The image of the LSFET array (reproduced below) also shows grading near the source and drain and in wells.

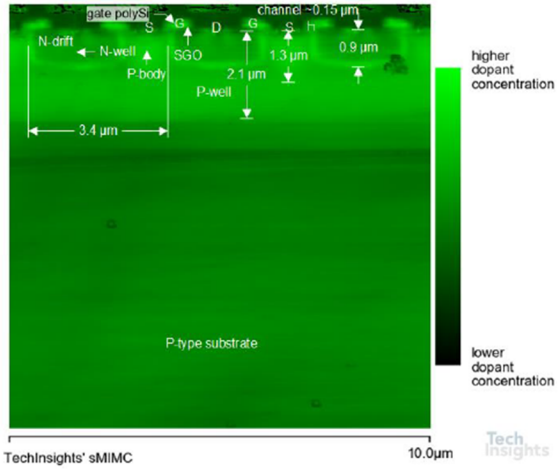
MP9502 Die LSFET Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the LSFET array show the use of a P-type body region, shallower N-drift/N-well in the drain region, and NBL is absent in the LSFET array.
- The P-well is ~2.1 µm deep, the P-body is ~1.3 µm deep, while the drain N-drift/N-well is ~0.9 µm deep, shallower than 1.2 µm observed in the HSFET array.
- Both HSFET and LSFET array likely share the P-well and P-body masks, but use different mask for drain drift region.
- The effective channel length defined by dopant boundary is estimated to be ~0.15 µm in the LSFET array.



Array_2_040622155352_PRODUCT_FRW_10.0u_512p_400973.png

LSFET Array – SCM Cross-Section A-A



Array_2_040622155352_SMIMC_FRW_10.0u_512p_400973.png

LSFET Array – sMIM-C Cross-Section A-A

2

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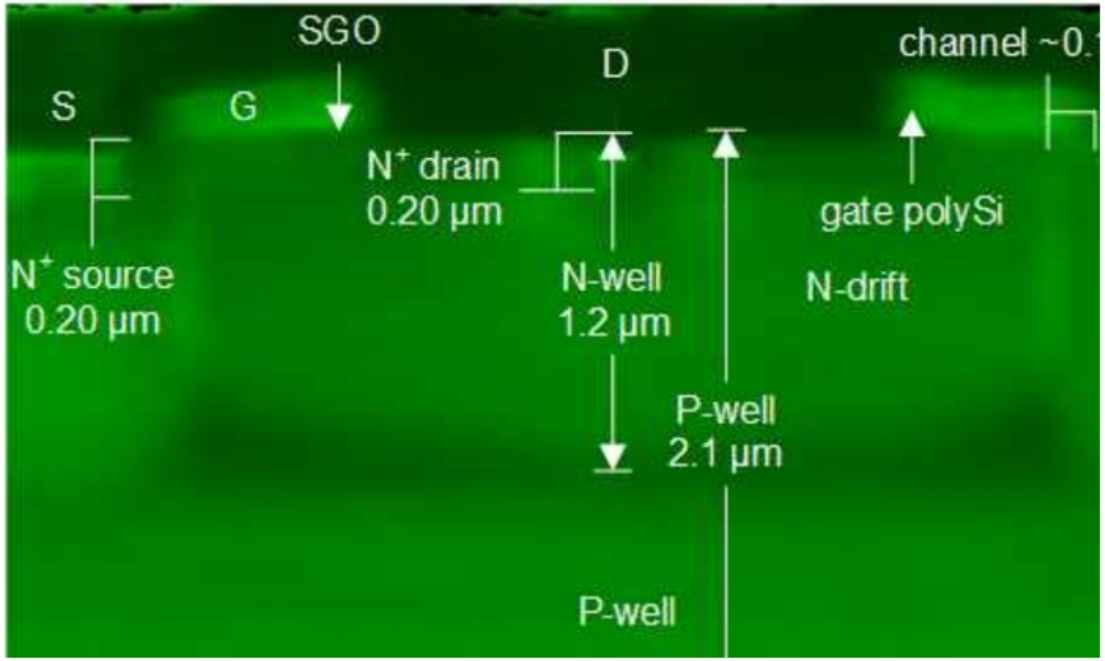
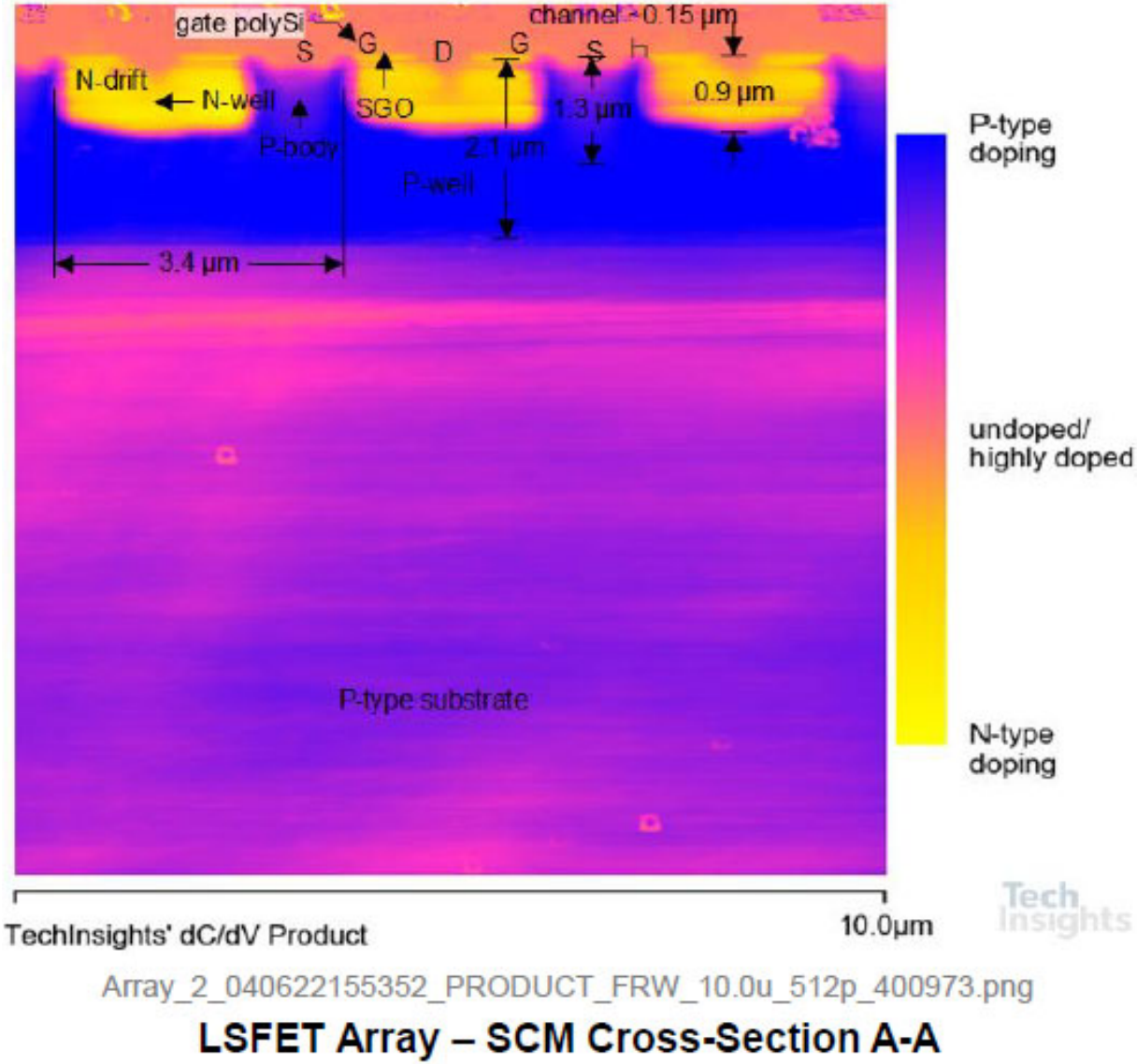
MP86905 Supplemental Report at 2.

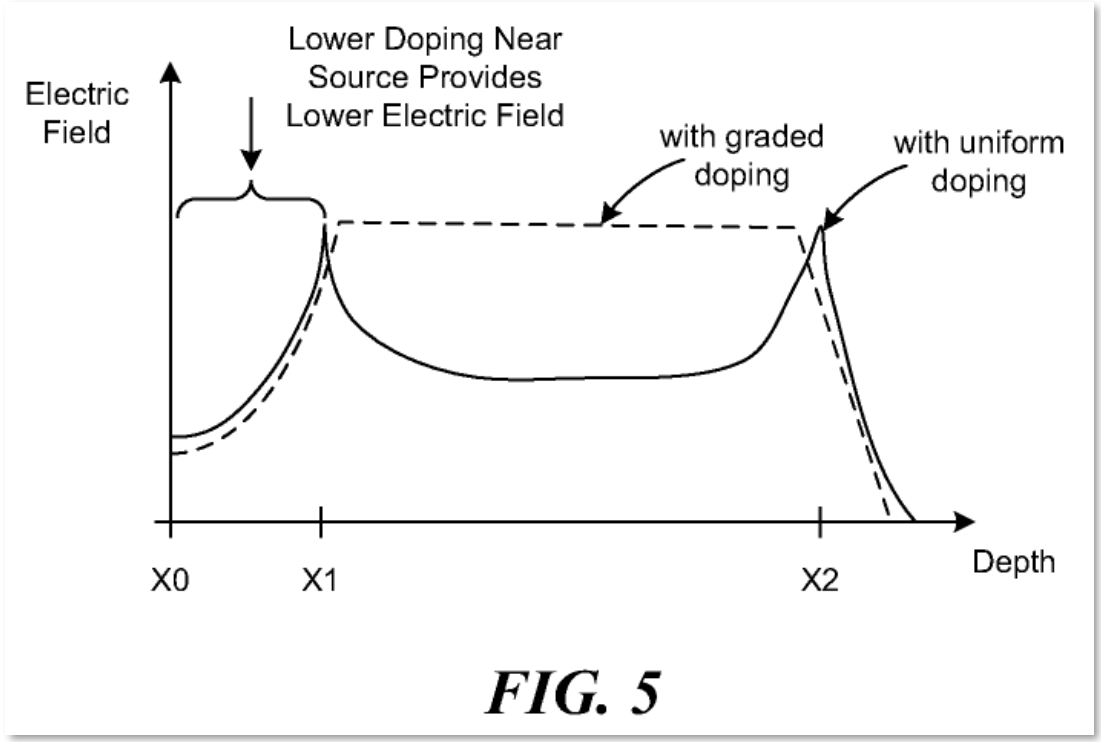
(Zoomed in near active regions on image from page 43)



MP86905 Report at 43.



MP86905 Report at 43.

	Additionally, MPS' annual report states that it seeks patent protection based on its product designs designs: "In general, we have elected to pursue patent protection for aspects of our circuit and device designs that we believe are patentable." *See* MPS "2021 ANNUAL REPORT ON FORM 10-K" at 4. Therefore, the purported inventions described in MPS's patents are an indication of how its products operate. The descriptions of MPS's purported inventions in its patent applications confirm that its products meet this limitation. For example, Figure 5 of MPS U.S. Patent No. 8,704,292 (below) clearly shows the use of graded dopants in active and well regions for the purposes of creating electric fields to aid carrier movement. The patent recites that "The dashed line in FIG.5 shows a uniform electric field distribution associated with an example drift region doping profile."  ***FIG. 5***
2. The semiconductor device of claim 1, wherein the substrate is a	Upon information and belief, the substrate of the semiconductor device of the MPS Accused Products is a p-type substance, as discussed above and shown in SCM/sMIM analysis above.

<table>
<tr><td>p-type substrate.</td><td></td></tr>
<tr><td>4. The semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.</td><td>Upon information and belief, the substrate of the MPS Accused Products has epitaxial silicon on top of a nonepitaxial substrate. For example, the device summary shown below includes an upper epitaxy layer.

Device Summary

▪ This report presents a Power Essentials analysis of the MPS MP86905 silicon (Si)-based power management IC (PMIC). The MP86905 is a monolithic half-bridge with built-in internal power MOSFETs and gate drivers and is ideally suited for multi-phase buck regulators. It offers 50 A continuous output current over a wide 4.5 V to 16 V operating input range [2].
▪ The MP86905 comprises a single die with MP9502 die markings, which are encapsulated in a 23-pin flip-chip quad-flat-no-lead (FC-QFN) package with likely copper (Cu) bumping directly to the leadframe.
▪ The MP9502 die substrate is ~155 µm thick including the upper epitaxy layer and uses Bipolar-CMOS-DMOS (BCD) technology. It features a single layer of polysilicon in the analyzed regions, three aluminum (Al) metal layers, tungsten (W) contacts and vias, cobalt silicide (CoSi) at the source, drain, and polysilicon contact regions. The pre-metal dielectric (PMD) uses silicon oxide (SiO) layers, while the inter-metal dielectric (IMD) layers uses oxide as well. Isolation structures include shallow trench isolation (STI) in the logic region.
▪ One group of high side MOSFET (HSFET) array and two groups of low side MOSFET (LSFET) array are used on the die. The structure and dopants of the HS/LS FET arrays are analyzed. Dopant analysis in the HS/LS FET array region shows the use of a P-type substrate, an N-type buried layer (NBL), a N-drift/N-well layer and a P-well layer.
▪ The stepped-gate-oxide (SGO) is used in the LDMOS devices on this die. The use of SGO allows a reduction of on-resistance (Ron) compared with the conventional STI LDMOS [3].
▪ The HSFET is arranged in a one-dimensional (1D) array with a ~4.0 µm drain-to-drain pitch and ~0.66 µm total polysilicon gate length, while the LSFET is arranged with ~3.4 µm drain-to-drain pitch and ~0.60 µm total polysilicon gate length in total.
▪ In the logic region, the minimum observed gate length is 0.40 µm on a 0.86 µm contacted gate pitch, indicating the use of likely 0.18 µm process generation with relaxed feature dimensions.

<table><tr><td>Manufacturer</td><td>Monolithic Power Systems</td></tr><tr><td>Part number</td><td>MP86905</td></tr><tr><td>Foundry</td><td>Unknown</td></tr><tr><td>Type</td><td>PMIC</td></tr><tr><td>Date code</td><td>H39 (week 39 of 2017)</td></tr><tr><td>Package type</td><td>23-pin FC-QFN</td></tr><tr><td>Package markings</td><td>MPSH39
M86905
54U403</td></tr><tr><td>Package dimensions</td><td>3.97 mm × 3.97 mm × 0.88 mm (thick)</td></tr><tr><td>Die markings</td><td>MP9502 2013
<MPS logo></td></tr><tr><td>Die size (whole die)</td><td>3.38 mm × 3.14 mm (10.61 mm²)</td></tr><tr><td>Die size (edge seal)</td><td>3.36 mm × 3.12 mm (10.48 mm²)</td></tr><tr><td>Minimum measured transistor gate length/pitch</td><td>0.40 µm/0.86 µm</td></tr><tr><td>Process generation</td><td>Likely 0.18 µm process generation with relaxed feature dimensions</td></tr><tr><td>Feature measured to determine process generation</td><td>Contacted gate pitch, use of CoSi contacts, STI isolation</td></tr><tr><td>Maximum voltage [2]</td><td>18 V</td></tr></table>
rary
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Insights Inc
Tech Insights</td></tr>
<tr><td>5. The semiconductor device of claim 1, wherein the first active</td><td>The MPS Accused Products meet this limitation. See above at Claim 2.</td></tr>
</table>

region and second active region contain one of either p-channel and n-channel devices.	
6. The semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant.	The MPS Accused Products meet this limitation. As shown above, the sources and drains are n-doped and therefore the device is p-channel. The first and second active regions accordingly contains p-channel devices. *See* Tech Insights Report images reproduced above at Claim 1, Element 2.
7. The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.	The MPS Accused Products meet this limitation. The first active region and second active region have n-type dopant and contain p-channel devices in n-wells. The wells have graded dopants. *See* Tech Insights Report images reproduced above at Claim 1, Element 2 annotating "n-wells."

8. The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.	Upon information and belief, the graded dopant is fabricated with an ion implantation process. For example, ion implantation is the prevalent process for implementing doping in semiconductor devices, and is believed to be used for the MPS's Accused Products. MPS's recent patent applications reference forming N regions and P regions by ion implantation. Information about the fabrication process for the MPS Accused Products, including usage of an ion implantation process, is in the possession of Defendant and is expected to be obtained through discovery.
[Claim 9, Preamble] A semiconductor device, comprising:	The MPS Accused Products meet this limitation. *See* above at Claim 1, Elements 1-3.
[Claim 9, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The MPS Accused Products meet this limitation. *See* above at Claim 1, Element 1.
[Claim 9, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within	The MPS Accused Products meet this limitation. *See* above at Claim 1, Element 2. Upon information and belief, transistors can be formed in the surface of the first active region. Details regarding formation of transistors are in the possession of Defendant and are expected to be obtained through discovery.

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

which transistors can be formed in the surface thereof;	
[Claim 9, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	The MPS Accused Products meet this limitation. *See* above at Claim 1, Element 3. Upon information and belief, transistors can be formed in the surface of the second active region. Details regarding formation of transistors are in the possession of Defendant and are expected to be obtained through discovery.
[Claim 9, Element 4] transistors formed in at least one of the first active region or second active region; and	The MPS Accused Products meet this limitation. *See* above at Claim 1, Element 4.
[Claim 9, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant	The MPS Accused Products meet this limitation. *See* above at Claim 1, Element 5.

concentration to aid carrier movement from the surface to the substrate.	
12. The semiconductor device of claim 9, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The MPS Accused Products meet this limitation. *See* above at Claim 4.
13. The semiconductor device of claim 9, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.	The MPS Accused Products meet this limitation. *See* above at Claim 5.
14. The semiconductor device of claim 9, wherein the first active region and second active region contain	The MPS Accused Products meet this limitation. *See* above at Claim 6.

either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant.	
15. The semiconductor device of claim 9, wherein the first active region and second active region are each separated by at least one isolation region.	Upon information and belief, the MPS Accused Products meet this limitation. *See* above at Claim 7.
16. The semiconductor device of claim 9, wherein the graded dopant is fabricated with an ion implantation process.	Upon information and belief, the MPS Accused Products meet this limitation. *See* above at Claim 8.
17. The semiconductor device of claim 1, wherein the first and second active	The MPS Accused Products meet this limitation. *See* above at Claim 1, Elements 2-3.

regions are formed adjacent the first surface of the substrate.	
18. The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring a source, a drain, a gate and a channel region.	The MPS Accused Products meet this limitation. As discussed above for Claim 1, the MPS Accused Products include first and second active regions. Upon information and belief, CMOS transistors formed in the first and second active regions, the CMOS transistors requiring a source, a drain, a gate, and a channel region. Details regarding transistors used are in the possession of Defendant and are expected to be obtained through discovery.

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

U.S. Patent No. 10,734,481	Exemplary Accused Product MPS 86905 Intelli-Phase Solution with integrated HS/LS-FETs and Driver
[Claim 1, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the MPS Accused Products constitute and are incorporated into semiconductor devices. This chart includes exemplary information regarding a representative example of the MPS Semiconductor 86905 Intelli-Phase Solution with integrated HS/LS-FETs and Driver ("86905"). The 86905 was analyzed in the below referenced report from Tech Insights. MPS MP86905 Intelli-PhaseTM Solution with Integrated HS/LS-FETs and Driver Power Essentials Summary ("MP86905 Report"), *available at* https://library.techinsights.com/search/device-details?tab=reports&id=PEF-2202-801&genealogyCode=MPS-MP9502. The 86905 was also analyzed in a supplemental report from Tech Insights ("MP86905 Supplemental Report"). *See* Exhibit 8 (Supplemental Report for PEF-2202-801). The complete reports are hereby incorporated by reference into each and every claim and claim element discussed. Selected pages are reproduced herein to aid in understanding. The MPS 86905 is representative of the MPS Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other MPS Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '481 patent (and the other asserted patents). For example, the other MPS Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '481 patent (and the other asserted patents). Similarly, the other MPS Accused Products (including MPS Accused Products) would have been designed in a similar manner as the MPS 86905 for purposes of this claim chart to achieve such performance enhancements (e.g., on and off switching times). The claimed invention would have application in numerous types of MPS products, including switching converters and controllers, multi-phase controllers, power management integrated circuits, USB switches, load switches, MOFSET drivers, insolated gate drivers, digital isolators, isolated DC/DC converters, power modules, battery chargers and monitors, fuel gauges, stepper motor drivers, brushless DC pre-drivers, brushless DC motor controllers, brushed DC drivers, fan drivers, backlight drivers, audio drivers, analog-to-digital converters, angular position sensors, and current sensors, because such products would benefit from, among other things, improved switching time for transistors in the device. Therefore, upon information and belief the other MPS Accused Products contain similar features as the MPS 86905 transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other MPS Accused Products contain similar features as the MPS 86905, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery. The MPS Accused Products, of which MPS 86905 is one example, are semiconductor devices.

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

Device Summary

- This report presents a Power Essentials analysis of the MPS MP86905 silicon (Si)-based power management IC (PMIC). The MP86905 is a monolithic half-bridge with built-in internal power MOSFETs and gate drivers and is ideally suited for multi-phase buck regulators. It offers 50 A continuous output current over a wide 4.5 V to 16 V operating input range [2].
- The MP86905 comprises a single die with MP9502 die markings, which are encapsulated in a 23-pin flip-chip quad-flat-no-lead (FC-QFN) package with likely copper (Cu) bumping directly to the leadframe.
- The MP9502 die substrate is ~155 µm thick including the upper epitaxy layer and uses Bipolar-CMOS-DMOS (BCD) technology. It features a single layer of polysilicon in the analyzed regions, three aluminum (Al) metal layers, tungsten (W) contacts and vias, cobalt silicide (CoSi) at the source, drain, and polysilicon contact regions. The pre-metal dielectric (PMD) uses silicon oxide (SiO) layers, while the inter-metal dielectric (IMD) layers uses oxide as well. Isolation structures include shallow trench isolation (STI) in the logic region.
- One group of high side MOSFET (HSFET) array and two groups of low side MOSFET (LSFET) array are used on the die. The structure and dopants of the HS/LS FET arrays are analyzed. Dopant analysis in the HS/LS FET array region shows the use of a P-type substrate, an N-type buried layer (NBL), a N-drift/N-well layer and a P-well layer.
- The stepped-gate-oxide (SGO) is used in the LDMOS devices on this die. The use of SGO allows a reduction of on-resistance (Ron) compared with the conventional STI LDMOS [3].
- The HSFET is arranged in a one-dimensional (1D) array with a ~4.0 µm drain-to-drain pitch and ~0.66 µm total polysilicon gate length, while the LSFET is arranged with ~3.4 µm drain-to-drain pitch and ~0.60 µm total polysilicon gate length in total.
- In the logic region, the minimum observed gate length is 0.40 µm on a 0.86 µm contacted gate pitch, indicating the use of likely 0.18 µm process generation with relaxed feature dimensions.

Manufacturer	Monolithic Power Systems
Part number	MP86905
Foundry	Unknown
Type	PMIC
Date code	H39 (week 39 of 2017)
Package type	23-pin FC-QFN
Package markings	MPSH39 M86905 54U403
Package dimensions	3.97 mm × 3.97 mm × 0.88 mm (thick)
Die markings	MP9502 2013 <MPS logo>
Die size (whole die)	3.38 mm × 3.14 mm (10.61 mm²)
Die size (edge seal)	3.36 mm × 3.12 mm (10.48 mm²)
Minimum measured transistor gate length/pitch	0.40 µm/0.86 µm
Process generation	Likely 0.18 µm process generation with relaxed feature dimensions
Feature measured to determine process generation	Contacted gate pitch, use of CoSi contacts, STI isolation
Maximum voltage [2]	18 V

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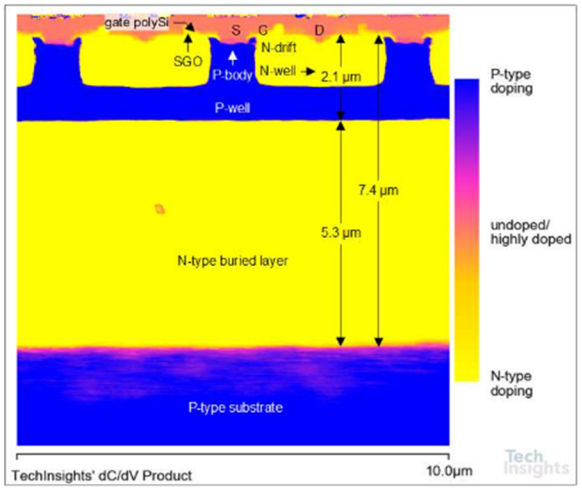
MP86905 Report at 5.

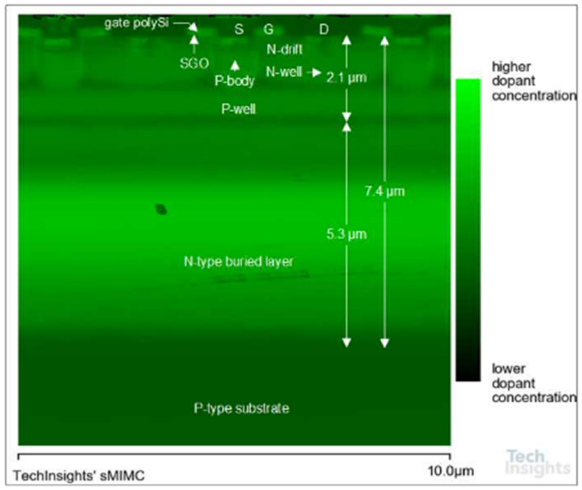
MP9502 Die HSFET Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the HSFET array show the use of a P-type body region, N-type drift region, and a higher-doped N-well at the drain region.
- The P-well layer starts ~2.1 µm from the front surface, while the NBL measures ~5.3 µm thick and reaches ~7.4 µm deep.
- NBL seems to have two regions of higher-doped lower portion and lower-doped upper portion in the Si body.



Array_040522164608_PRODUCT_FRW_10.0u_512p_400973.png

HSFET Array – SCM Cross-Section A-A



Array_040522164608_SMIMC_FRW_10.0u_512p_400973.png

HSFET Array – sMIM-C Cross-Section A-A

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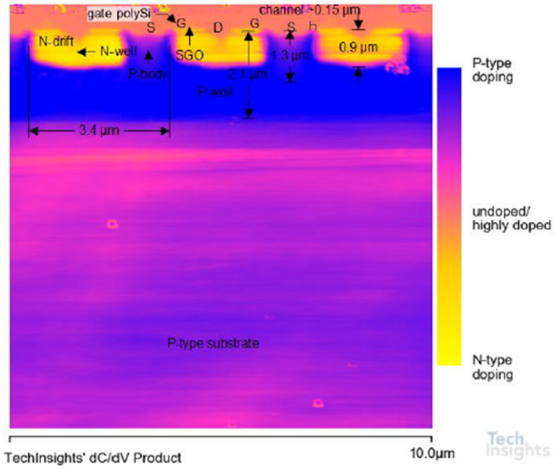
MP86905 Report at 42.

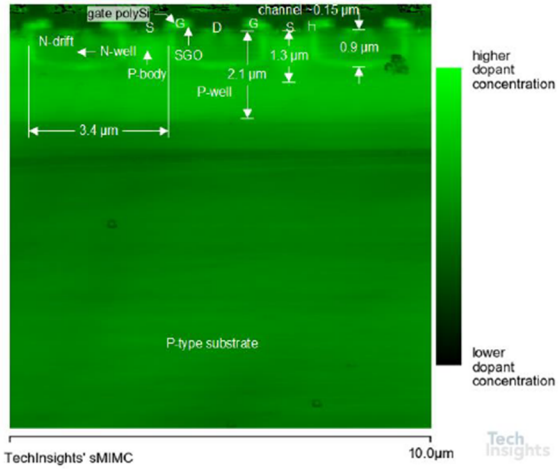
MP9502 Die LSFET Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the LSFET array show the use of a P-type body region, shallower N-drift/N-well in the drain region, and NBL is absent in the LSFET array.
- The P-well is ~2.1 µm deep, the P-body is ~1.3 µm deep, while the drain N-drift/N-well is ~0.9 µm deep, shallower than 1.2 µm observed in the HSFET array.
- Both HSFET and LSFET array likely share the P-well and P-body masks, but use different mask for drain drift region.
- The effective channel length defined by dopant boundary is estimated to be ~0.15 µm in the LSFET array.



Array_2_040622155352_PRODUCT_FRW_10.0u_512p_400973.png

LSFET Array – SCM Cross-Section A-A



Array_2_040622155352_SMIMC_FRW_10.0u_512p_400973.png

LSFET Array – sMIM-C Cross-Section A-A

2

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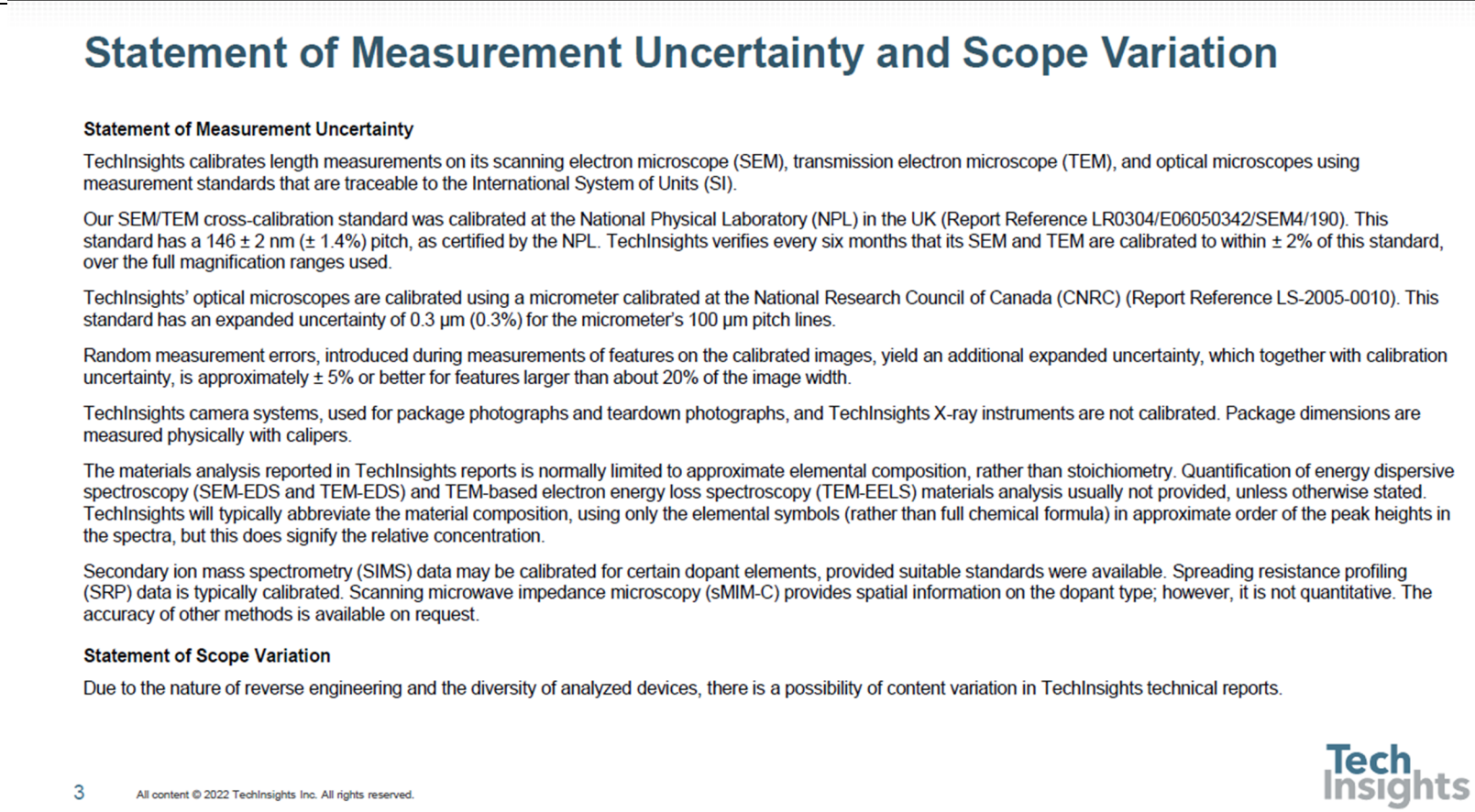
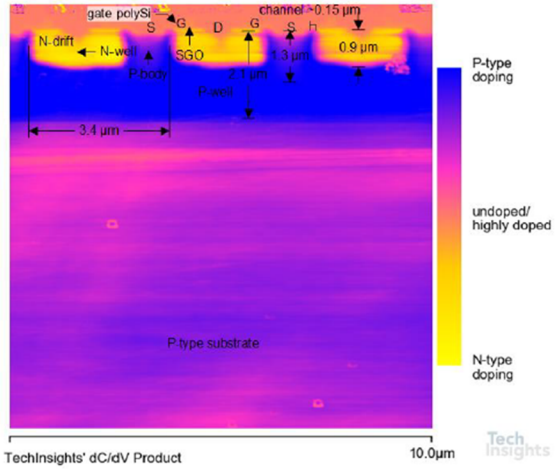
MP86905 Supplemental Report at 2.

	 MP86905 Supplemental Report at 3.
[Claim 1, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The MPS Accused Products include/comprise a semiconductor device comprising a substrate of a first doping type at a first doping level having first and second surfaces. For example, analysis of an exemplary MPS Accused Product (the MPS 86905 discussed above) reveals the presence of such a substrate. For example, the MPS 86905 discussed above for Claim 1, Preamble, was imaged using scanning electron microscopy (SEM) scanning capacitance/microwave impedance microscopy (SCM/SMIM) analysis.

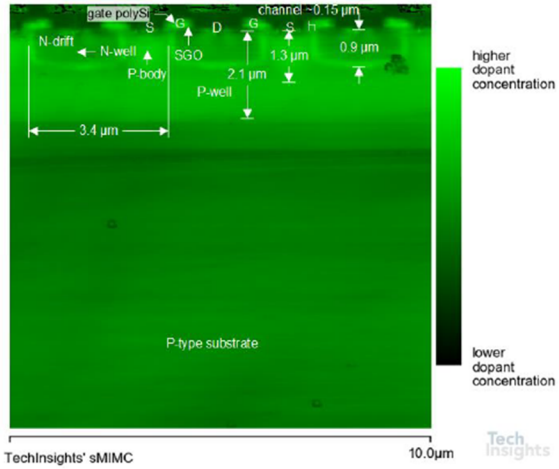
MP9502 Die LSFET Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the LSFET array show the use of a P-type body region, shallower N-drift/N-well in the drain region, and NBL is absent in the LSFET array.
- The P-well is ~2.1 µm deep, the P-body is ~1.3 µm deep, while the drain N-drift/N-well is ~0.9 µm deep, shallower than 1.2 µm observed in the HSFET array.
- Both HSFET and LSFET array likely share the P-well and P-body masks, but use different mask for drain drift region.
- The effective channel length defined by dopant boundary is estimated to be ~0.15 µm in the LSFET array.



Array_2_040622155352_PRODUCT_FRW_10.0u_512p_400973.png

LSFET Array – SCM Cross-Section A-A



Array_2_040622155352_SMIMC_FRW_10.0u_512p_400973.png

LSFET Array – sMIM-C Cross-Section A-A

2

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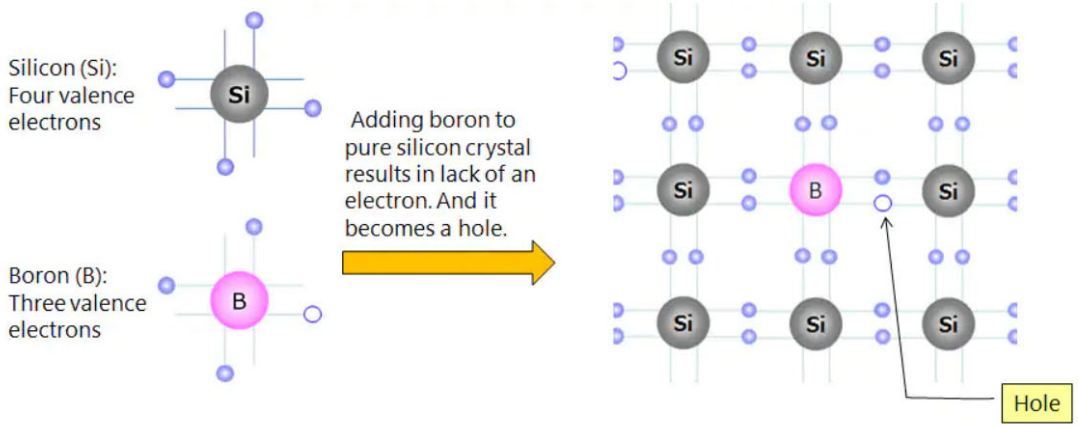
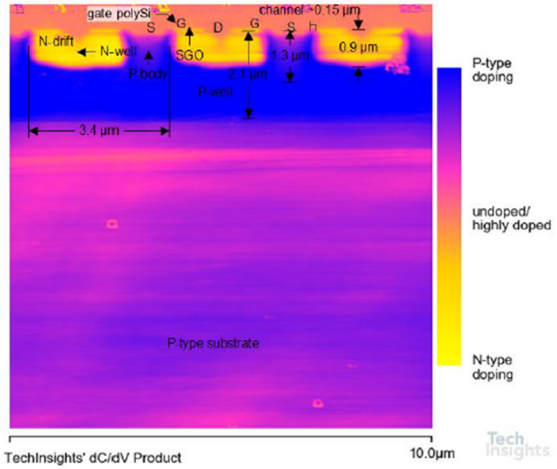
MP86905 Supplemental Report at 2.

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

	What is a p-type Semiconductor? A p-type semiconductor is an intrinsic semiconductor doped with boron (B) or indium (In). Silicon of Group IV has four valence electrons and boron of Group III has three valence electrons. If a small amount of boron is doped to a single crystal of silicon, valence electrons will be insufficient at one position to bond silicon and boron, resulting in holes* that lack electrons. When a voltage is applied in this state, the neighboring electrons move to the hole, so that the place where an electron is present becomes a new hole, and the holes appear to move to the "–" electrode in sequence.  * This hole is the carrier of a p-type semiconductor. *See* https://toshiba.semicon-storage.com/us/semiconductor/knowledge/e-learning/discrete/chap1/chap1-4.html#:~:text=A%20p%2Dtype%20semiconductor%20is,III%20has%20three%20valence%20electrons.
[Claim 1, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The MPS Accused Products, and products incorporating them, include/comprise a semiconductor device comprising a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed. For example, as shown in imagery from the Tech Insights Report, the exemplary MPS 86905 scanning capacitance/microwave impedance microscopy (SCM/SMIM) analysis includes a first active region disposed adjacent the first surface of the substrate. *See* below showing "HSFET Array," and toward the top the source ("S"), gate ("g") and drain ("drain") where the transistors are, underneath each of the annotations are active regions. *See also* below showing "LSFET Array."

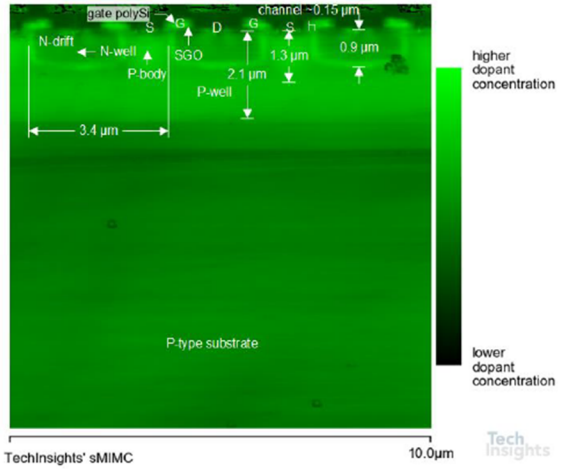
MP9502 Die LSFET Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the LSFET array show the use of a P-type body region, shallower N-drift/N-well in the drain region, and NBL is absent in the LSFET array.
- The P-well is ~2.1 µm deep, the P-body is ~1.3 µm deep, while the drain N-drift/N-well is ~0.9 µm deep, shallower than 1.2 µm observed in the HSFET array.
- Both HSFET and LSFET array likely share the P-well and P-body masks, but use different mask for drain drift region.
- The effective channel length defined by dopant boundary is estimated to be ~0.15 µm in the LSFET array.



Array_2_040622155352_PRODUCT_FRW_10.0u_512p_400973.png

LSFET Array – SCM Cross-Section A-A



Array_2_040622155352_SMIMC_FRW_10.0u_512p_400973.png

LSFET Array – sMIM-C Cross-Section A-A

2

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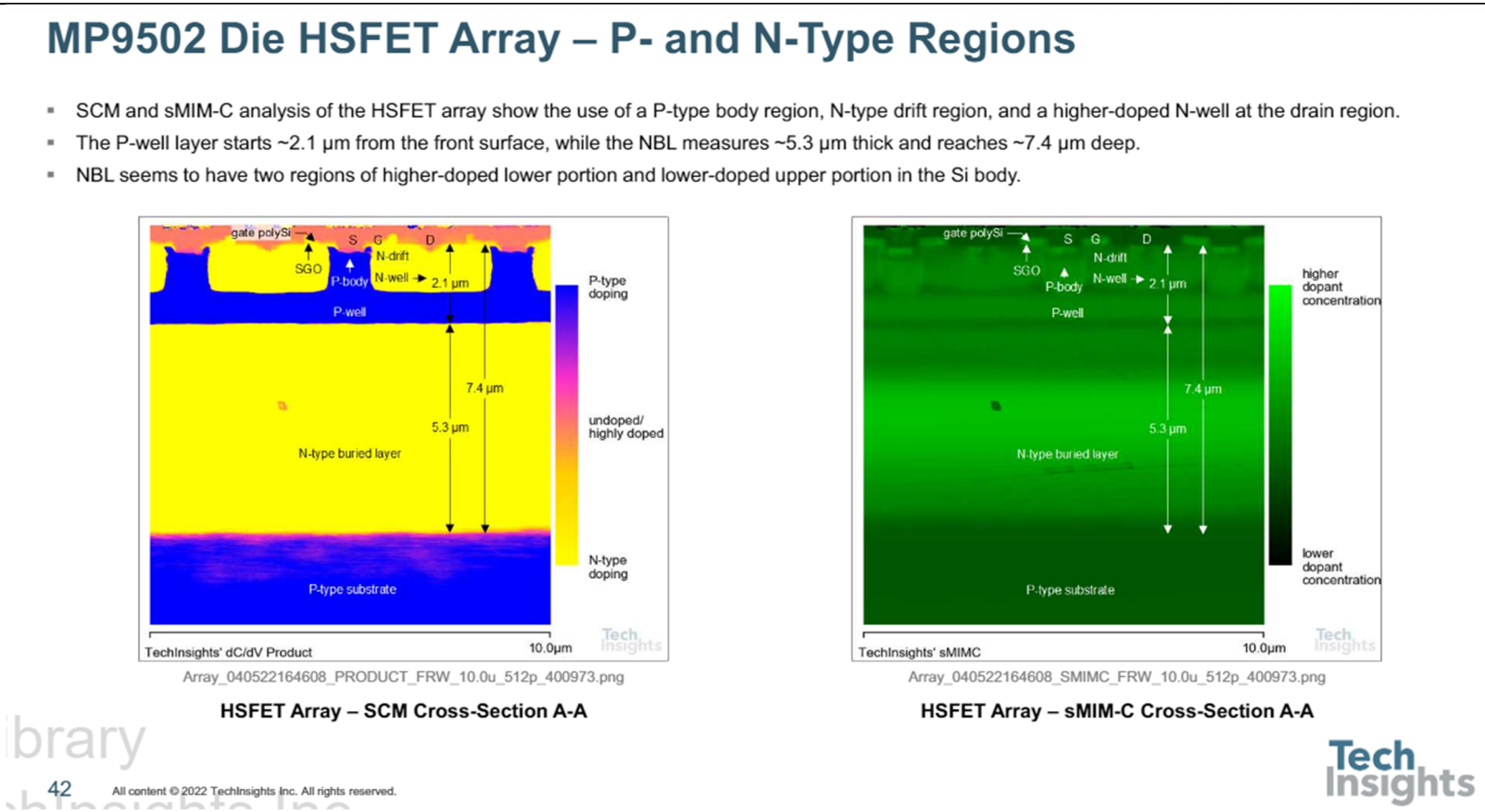
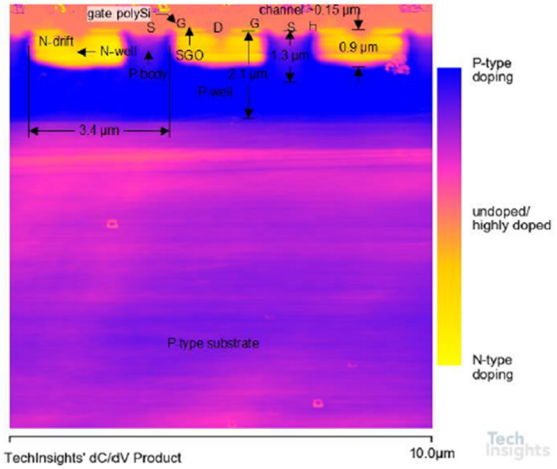
MP86905 Supplemental Report at 2.

	 MP86905 Report at 42.
[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active region	The MPS Accused Products include a semiconductor device comprising a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed. For example, the HSFET and LSFET arrays shown in the images reproduced at Claim 1, Element 2 shows multiple transistors with active regions.

and within which transistors can be formed;	
[Claim 1, Element 4] transistors formed in at least one of the first active region or second active region;	The MPS Accused Products include a semiconductor device comprising transistors formed in at least one of the first active region or second active region. *See* above at Preamble, Elements 2-3 (discussing the HSFET AND LSFET arrays).
[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate; and	The MPS Accused Products meet this limitation. *See* above at Element 1. For example, this is shown by the scanning capacitance/microwave impedance microscopy (SCM/sMIM) analysis. SCM/sMIM electrically characterizes the tested device and generates maps, which provide graphical representation of the dopant types and concentrations by measuring carrier movement as they are attracted to or repulsed by the probe. The SCM/SMIM maps taken from MPS Accused Products shown herein demonstrate differences in carrier concentration as a function of depth, which generate electric fields within the accused products. The contrast in the SMIM image is proportional to the capacitance of the sample under inspection, so that brighter green corresponds to higher dopant concentration, and darker green/black corresponds to lower dopant concentration. Likewise, the SCM images above show doping concentration and doping type as indicated in the legends to the right. Zooming in on the sMIM-C image taken from page 43 of the Tech Insights report clearly shows vertical dopant grading in the active regions surounding the source, gate, and drain. The image of the LSFET array (reproduced below) also shows grading near the source and drain and in wells.

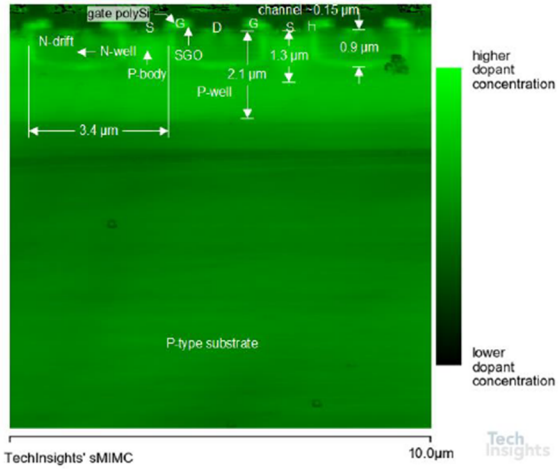
MP9502 Die LSFET Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the LSFET array show the use of a P-type body region, shallower N-drift/N-well in the drain region, and NBL is absent in the LSFET array.
- The P-well is ~2.1 µm deep, the P-body is ~1.3 µm deep, while the drain N-drift/N-well is ~0.9 µm deep, shallower than 1.2 µm observed in the HSFET array.
- Both HSFET and LSFET array likely share the P-well and P-body masks, but use different mask for drain drift region.
- The effective channel length defined by dopant boundary is estimated to be ~0.15 µm in the LSFET array.



Array_2_040622155352_PRODUCT_FRW_10.0u_512p_400973.png

LSFET Array – SCM Cross-Section A-A



Array_2_040622155352_SMIMC_FRW_10.0u_512p_400973.png

LSFET Array – sMIM-C Cross-Section A-A

2

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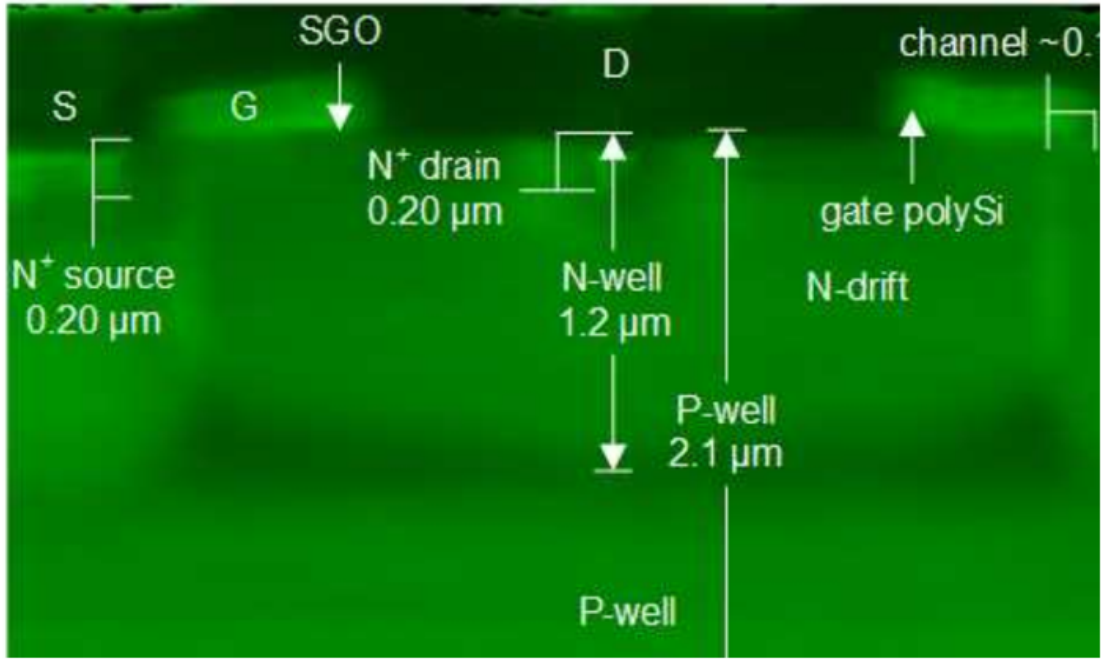
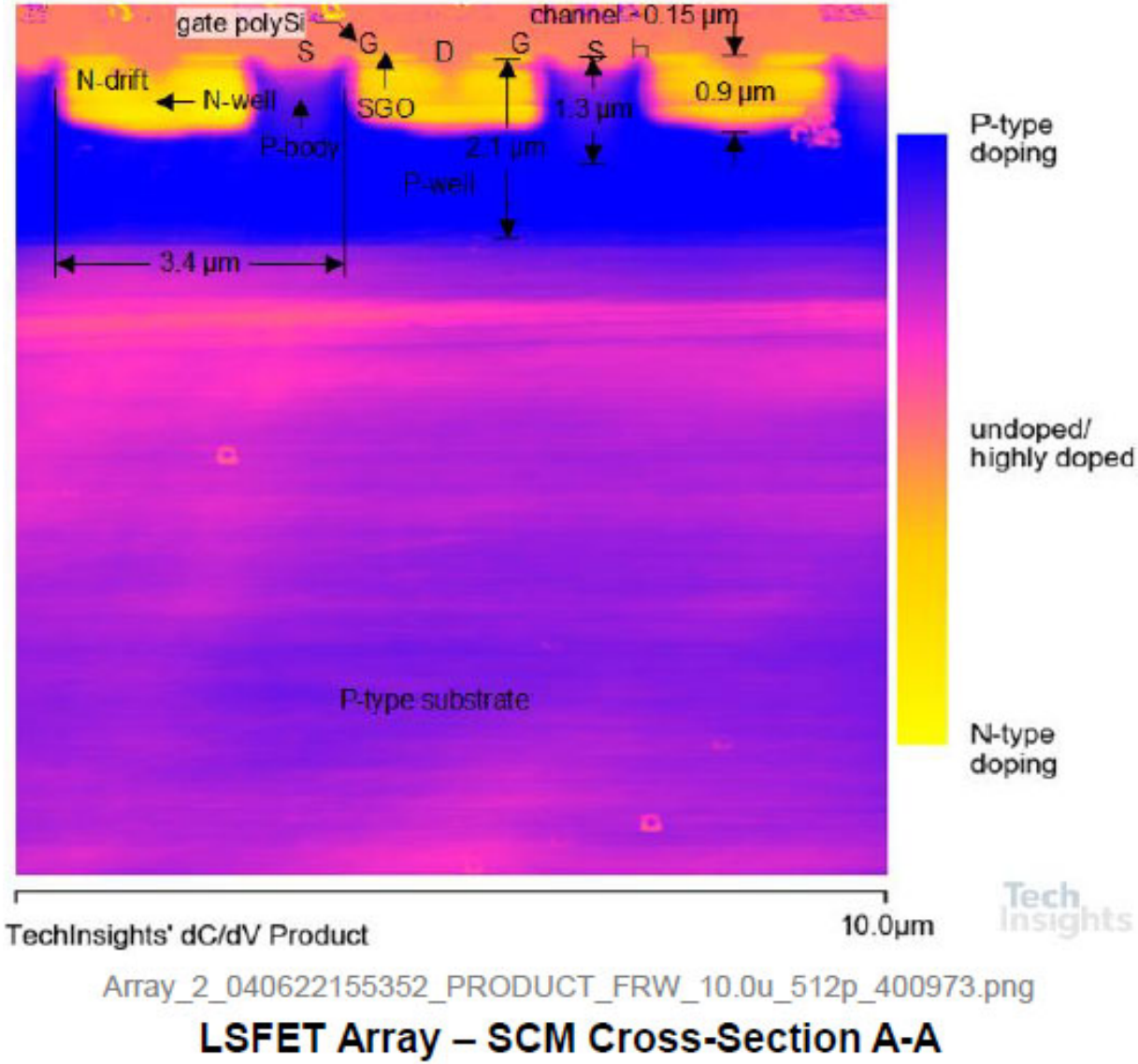
MP86905 Supplemental Report at 2.

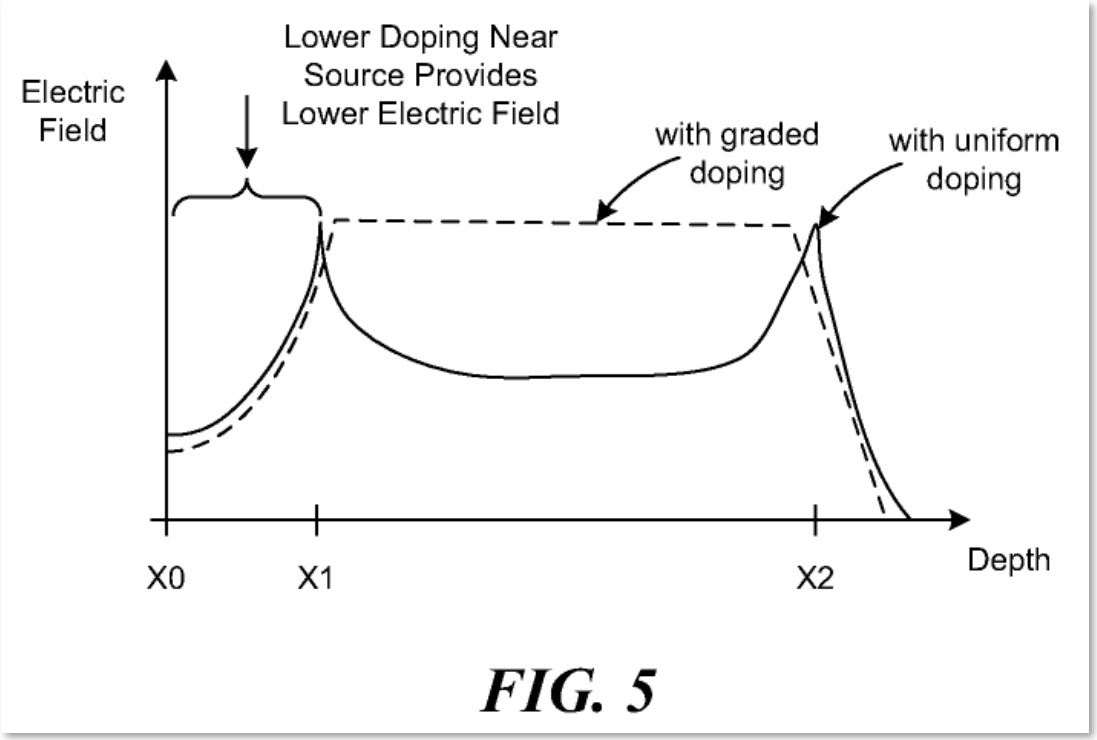
(Zoomed in near active regions on image from page 43)

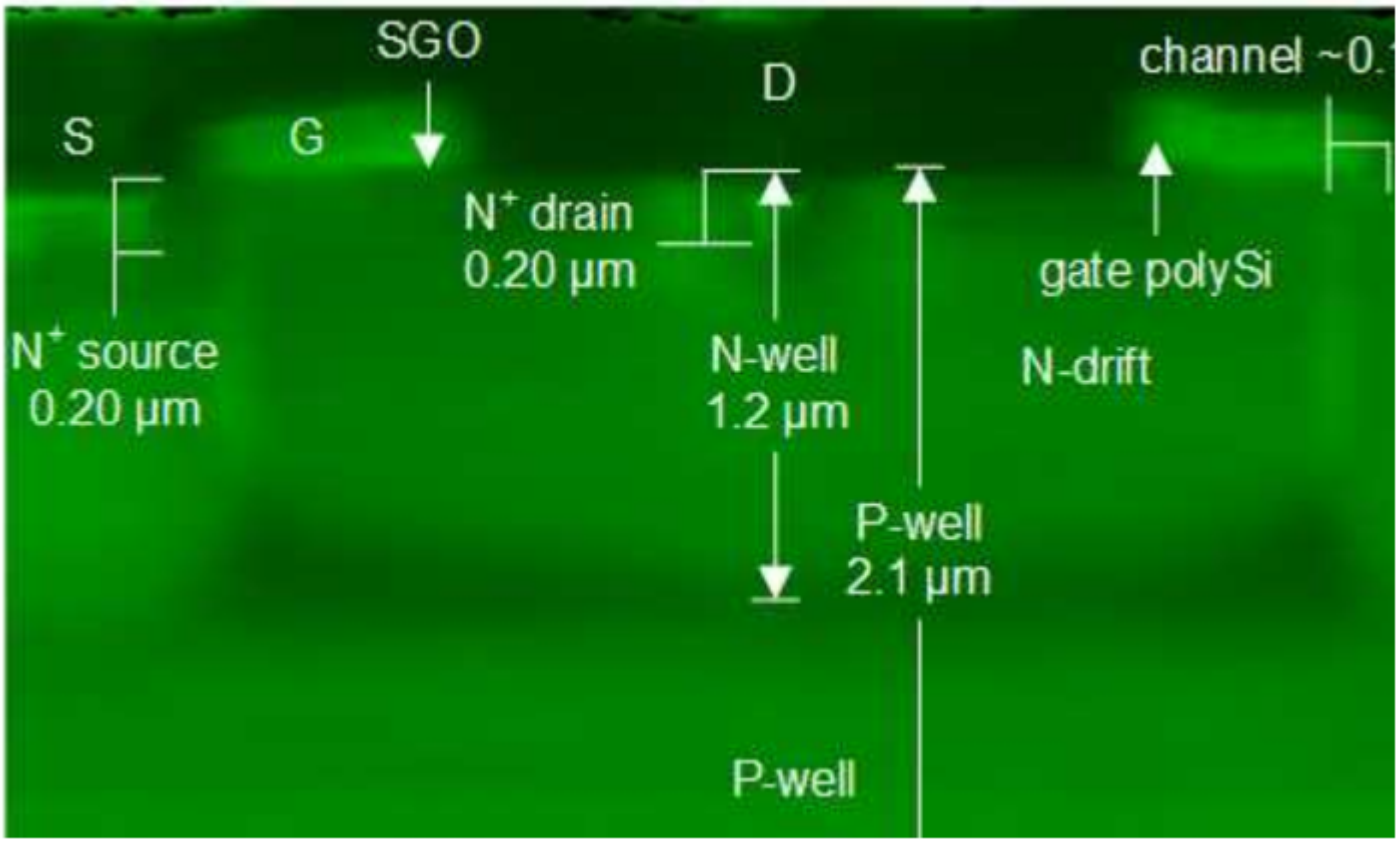


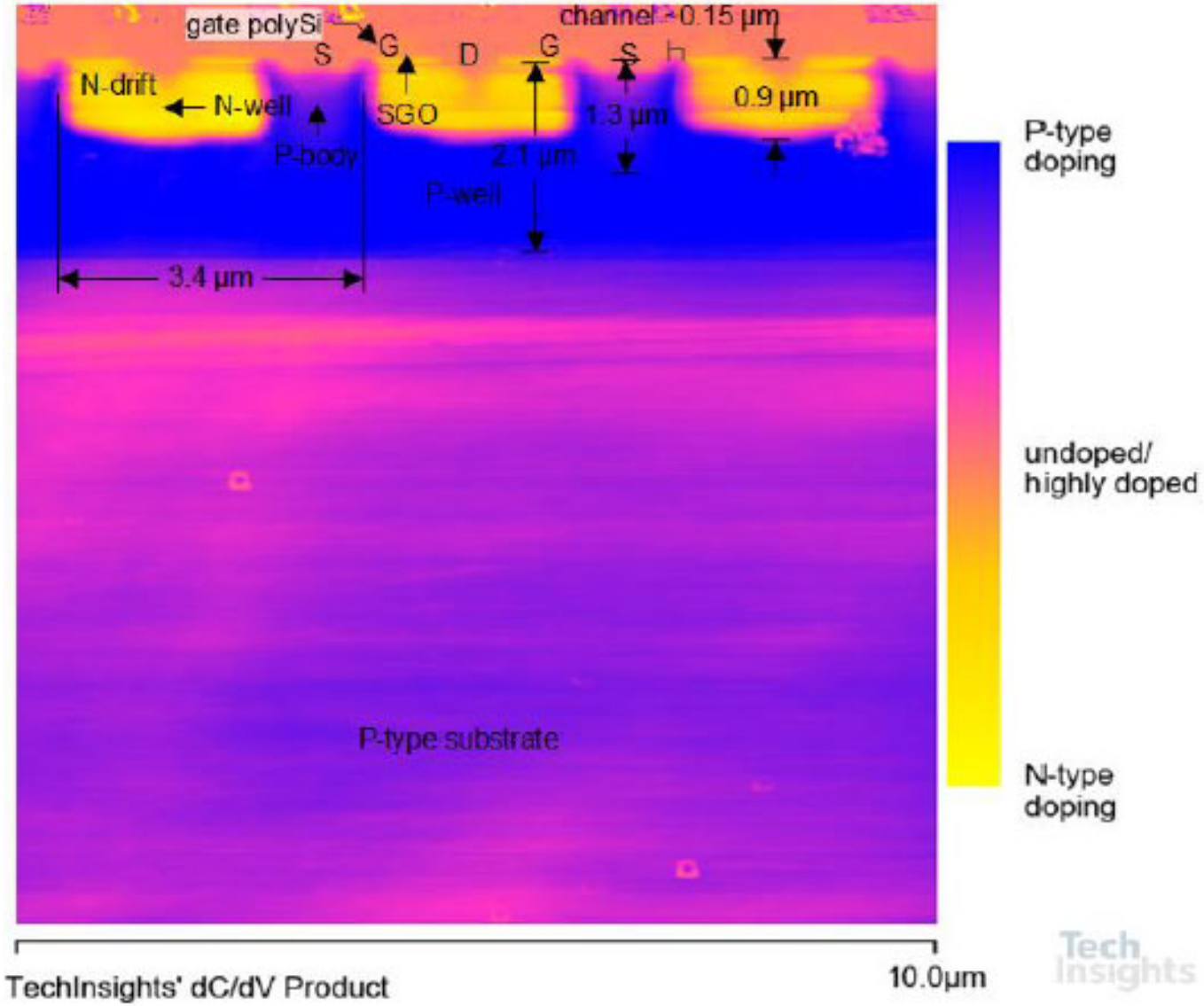
MP86905 Report at 43.



MP86905 Report at 43.

	Additionally, MPS' annual report states that it seeks patent protection based on its product designs designs: "In general, we have elected to pursue patent protection for aspects of our circuit and device designs that we believe are patentable." *See* MPS "2021 ANNUAL REPORT ON FORM 10-K" at 4. Therefore, the purported inventions described in MPS's patents are an indication of how its products operate. The descriptions of MPS's purported inventions in its patent applications confirm that its products meet this limitation. For example, Figure 5 of MPS U.S. Patent No. 8,704,292 (below) clearly shows the use of graded dopants in active and well regions for the purposes of creating electric fields to aid carrier movement. The patent recites that "The dashed line in FIG.5 shows a uniform electric field distribution associated with an example drift region doping profile."  *FIG. 5*
[Claim 1, Element 6] at	The MPS Accused Products include a semiconductor device comprising at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate. The images of the HSFET and LESFET arrays reproduced below (and above) clearly show dopant grading in the well regions. Likewise, Figure 5 from MPS's '292 patent

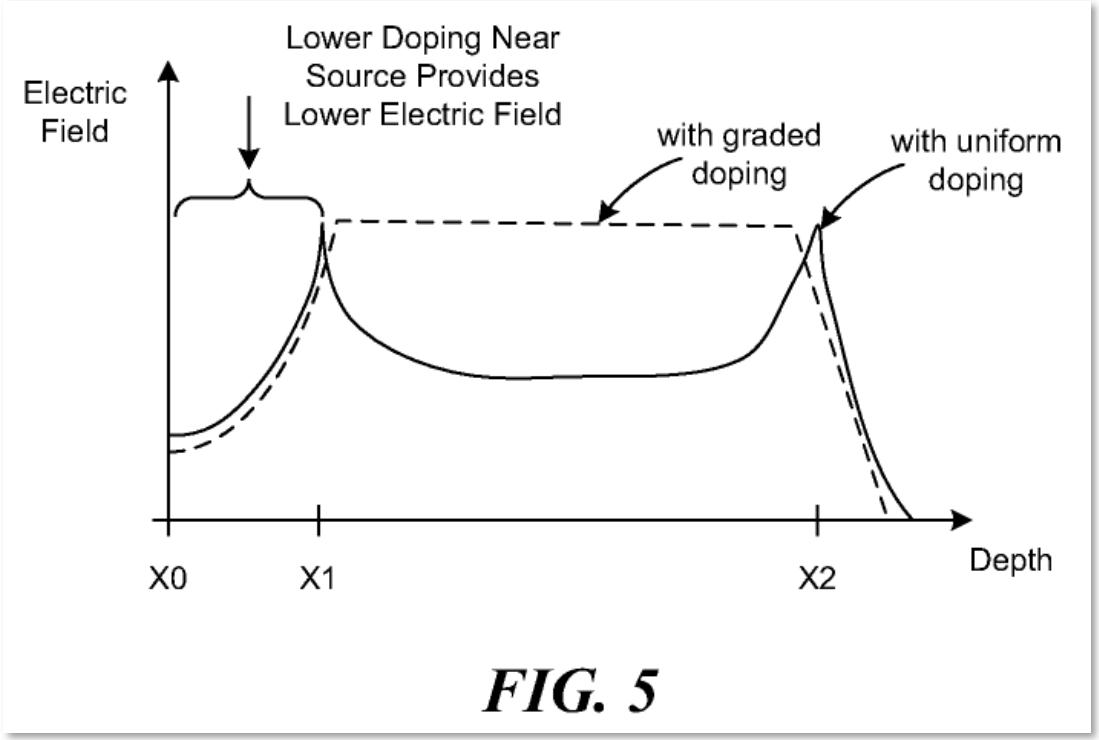
least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.	shows grading in a well region. (Zoomed in near active regions on image from page 43) 

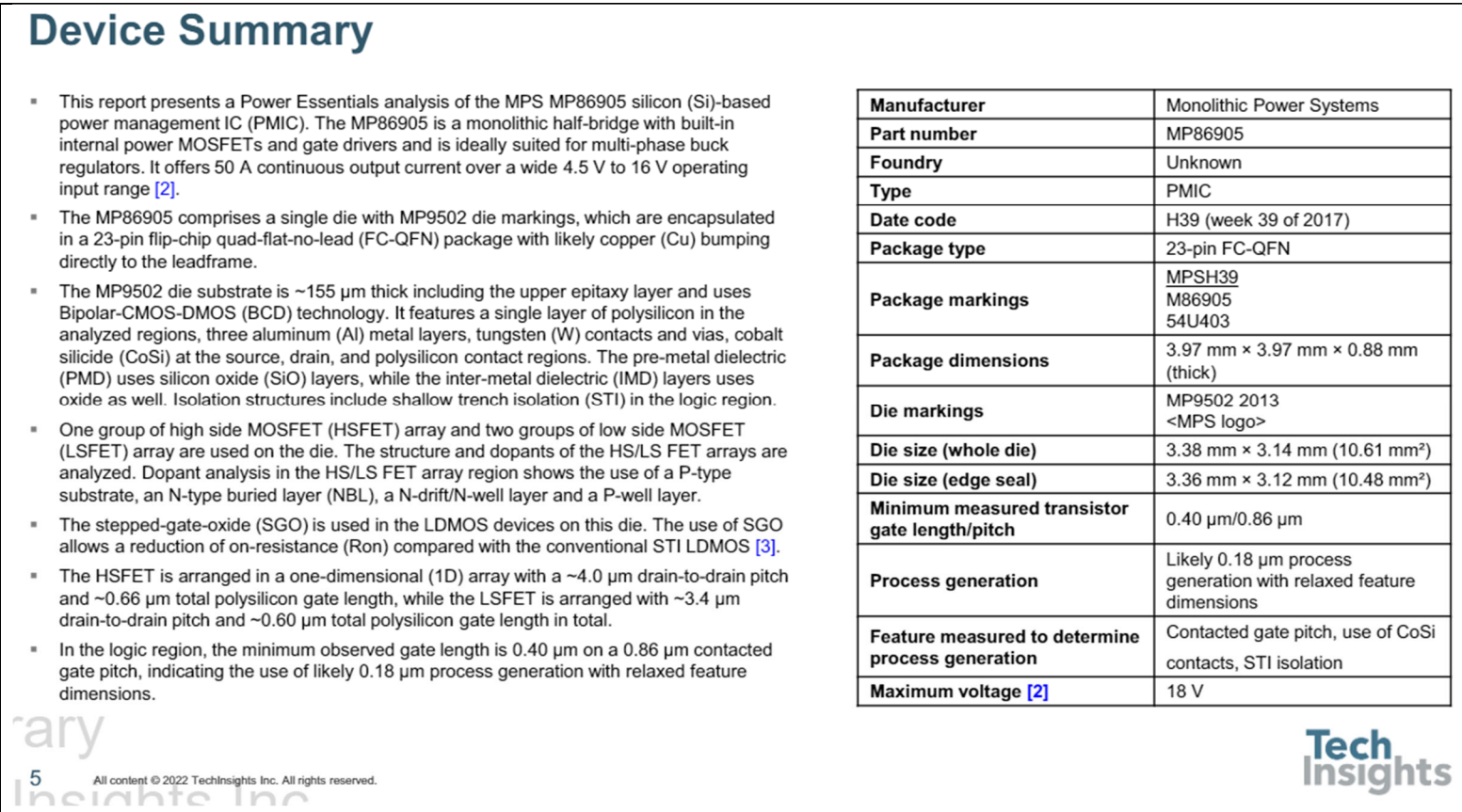


Array_2_040622155352_PRODUCT_FRW_10.0u_512p_400973.png

LSFET Array – SCM Cross-Section A-A

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

	 *FIG. 5*
2. The semiconductor device of claim 1, wherein the substrate is a p-type substrate.	Upon information and belief, the substrate of the semiconductor device of the MPS Accused Products is a p-type substance, as discussed above and shown in SCM/sMIM analysis above.
3. The semiconductor device of claim 1, wherein the substrate has	Upon information and belief, the substrate of the MPS Accused Products has epitaxial silicon on top of a nonepitaxial substrate. For example, the device summary shown below includes an upper epitaxy layer.

epitaxial silicon on top of a nonepitaxial substrate.	
4. The semiconductor device of claim 1, wherein the first active region and second active region contain one of either p-channel and n-channel devices.	The MPS Accused Products meet this limitation. *See* above at Claim 2.

5. The semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant.	The MPS Accused Products meet this limitation. As shown above, the sources and drains are n-doped and therefore the device is p-channel. The first and second active regions accordingly contains p-channel devices. *See* Tech Insights Report images reproduced above at Claim 1, Element 2.
6. The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.	The MPS Accused Products meet this limitation. The first active region and second active region have n-type dopant and contain p-channel devices in n-wells. The wells have graded dopants. *See* Tech Insights Report images reproduced above at Claim 1, Element 2 annotating "n-wells."
7. The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.	Upon information and belief, the graded dopant is fabricated with an ion implantation process. For example, ion implantation is the prevalent process for implementing doping in semiconductor devices, and is believed to be used for the MPS's Accused Products. MPS's recent patent applications reference forming N regions and P regions by ion implantation. Information about the fabrication process for the MPS Accused Products, including usage of an ion implantation process, is in the possession of Defendant and is expected to be obtained through discovery.
8. The semiconductor device of claim	The MPS Accused Products meet this limitation. *See* above at Claim 1, Elements 1-3.

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

1, wherein the first and second active regions are formed adjacent the first surface of the substrate.	
9. The semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The MPS Accused Products meet this limitation. As shown by the images obtained by SPM/sMIM anlysis (*see* above at Claim 1, Element 5), the MPS Accused Products show blocks of highly n-doped and p-doped wells.
13.The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring at least a source, a drain, a gate and a channel.	The MPS Accused Products meet this limitation. As discussed above for Claim 1, the MPS Accused Products include first and second active regions. Upon information and belief, CMOS transistors are formed in the first and second active regions, the CMOS transistors requiring a source, a drain, a gate, and a channel region. Details regarding transistors used are in the possession of Defendant and are expected to be obtained through discovery.
15. The semiconductor device of claim 1, wherein the device is a	The MPS Accused Products meet this limitation. *See* above at Claim 3 (regarding epitaxy) and Claim 13 (regarding CMOS).

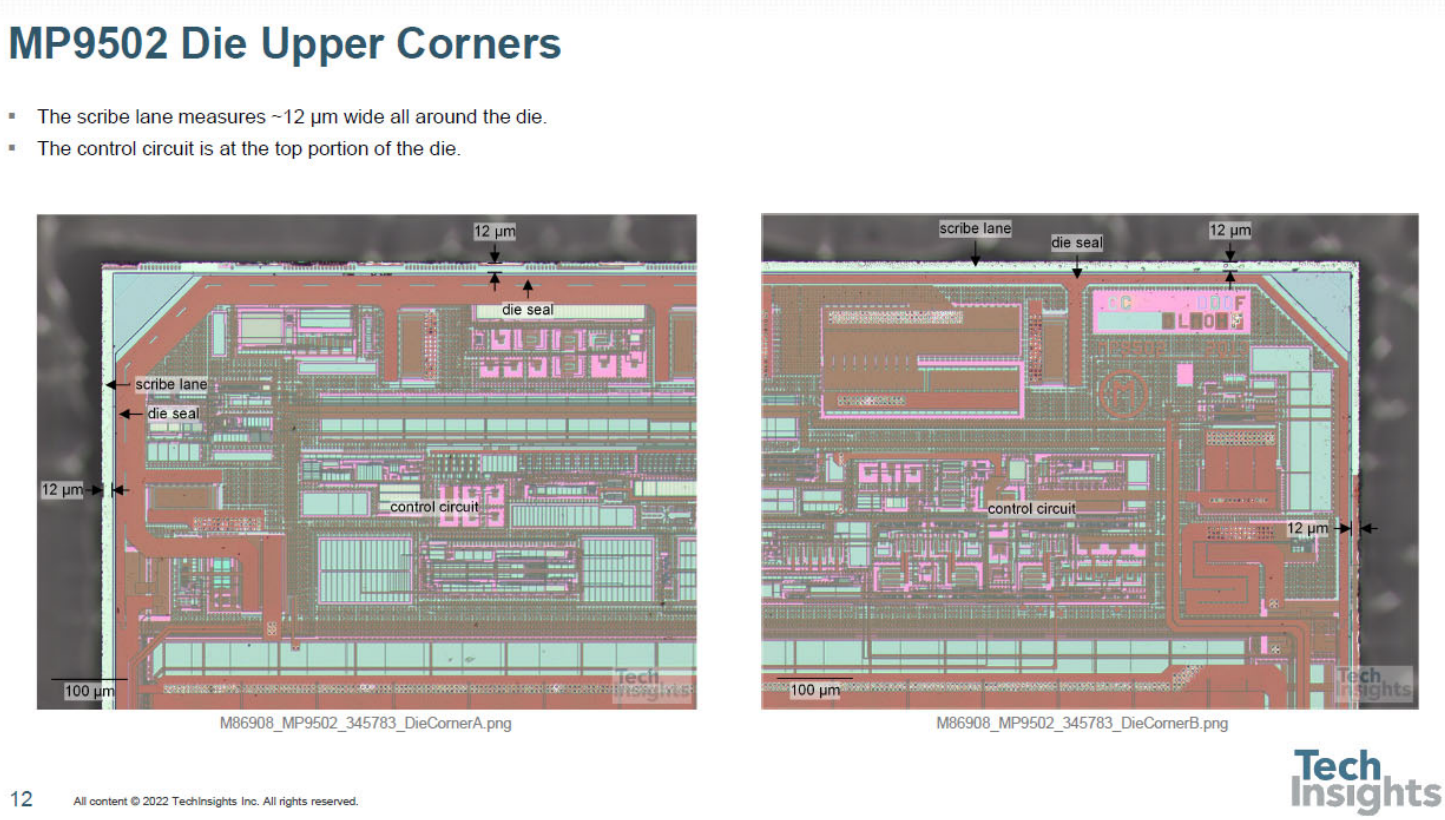
complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.	
17. The semiconductor device of claim 1, wherein the device is a logic device.	Upon information and belief, the MPS's Accused Products comprise a logic device. For example, the image below displays a "control circuit" region. 
[Claim 20, Preamble] A semiconductor	To the extent the preamble is a limitation, the MPS Accused Products include/comprise a semiconductor device. *See* above at Claim 1, Preamble.

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

device, comprising:	
[Claim 20, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The MPS Accused Products meet this limitation. *See* above at Claim 1, Element 1.
[Claim 20, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;	The MPS Accused Products meet this limitation. *See* above at Claim 1, Element 2. Upon information and belief, transistors can be formed in the surface of the first active region. Details regarding formation of transistors are in the possession of Defendant and are expected to be obtained through discovery.
[Claim 20, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be	The MPS Accused Products meet this limitation. Upon information and belief, transistors can be formed in the surface of the second active region. Details regarding formation of transistors are in the possession of Defendant and are expected to be obtained through discovery.

formed in the surface thereof;	
[Claim 20, Element 4] transistors formed in at least one of the first active region or second active region;	The MPS Accused Products meet this limitation. *See* above at Claim 1, Element 4.
[Claim 20, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate; and	The MPS Accused Products meet this limitation. *See* above at Claim 1, Element 5.
[Claim 20, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from	The MPS Accused Products meet this limitation. *See* above at Claim 6.

the first surface to the second surface of the substrate.	
22. The semiconductor device of claim 20, wherein the substrate is a p-type substrate.	The MPS Accused Products meet this limitation. See above at Claim 1, Element 2.
23. The semiconductor device of claim 20, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The MPS Accused Products meet this limitation. See above at Claim 3.
24. The semiconductor device of claim 20, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.	The MPS Accused Products meet this limitation. *See* above at Claim 4.
25.The semiconductor device of claim 20, wherein the first active region and second active region	The MPS Accused Products meet this limitation. *See* above at Claim 5.

contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	
26. The semiconductor device of claim 20, wherein the first active region and second active region are each separated by at least one isolation region.	The MPS Accused Products meet this limitation. *See* above at Claim 6.
27. The semiconductor device of claim 20, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The MPS Accused Products meet this limitation. *See* above at Claim 9.
31. The semiconductor device of claim 20, wherein the graded dopant is fabricated with an ion	The MPS Accused Products meet this limitation. *See* above at Claim 7.

implantation process.	
32. The semiconductor device of claim 20, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device.	The MPS Accused Products meet this limitation. *See* above at Claim 13.
34. The semiconductor device of claim 20, wherein the device is a logic device.	The MPS Accused Products meet this limitation. *See* above at Claim 17.

Exhibit A-3 to Greenthread's Complaint

U.S. Patent No. 11,121,222	Accused Products
[Claim 1, Preamble] A VLSI semiconductor device, comprising:	To the extent the preamble is a limitation, the MPS Accused Products include a VLSI semiconductor device. The MPS Semiconductor 86905 Intelli-Phase Solution with integrated HS/LS-FETs and Driver ("86905") discussed for claim 1 of Exhibit A-1 is a semiconductor device (*see* Exhibit A-1, Claim 1, Preamble) with transistors, and is a VLSI semiconductor device upon information and belief. Details regarding transistor count are in the possession of the Defendant and are expected to be obtained through discovery. This chart includes exemplary information regarding a representative example of the MPS Accused Products, the MPS 86905. The MPS 86905 is representative of the MPS Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other MPS Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '222 patent (and the other asserted patents). For example, the other MPS Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '222 patent (and the other asserted patents). Similarly, the other MPS Accused Products (including MPS Accused Products) would have been designed in a similar manner as the MPS 86905 for purposes of this claim chart because to achieve such performance enhancements (e.g., on and off switching times). Therefore, upon information and belief the other MPS Accused Products contain similar features as the MPS 86905 transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other MPS Accused Products contain similar features as the MPS 86905, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1] a substrate of a first doping type at a first doping level having a surface;	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 1.
[Claim 1, Element 2] a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 2.
[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 3.
[Claim 1, Element 4] transistors formed in at least one of the first	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 4.

Exhibit A-3 to Greenthread's Complaint

U.S. Patent No. 11,121,222	Accused Products
active region or second active region;	
[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 5. *See* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 1, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.	The MPS Accused Products meet this limitation. *See* Exhibit A-2, Claim 1, Element 6. Upon information and belief, at least some of the transistors form digital logic of the VLSI semiconductor device. For example, transistors are commonly used to implement digital logic, e.g., for controlling access to memory components/functionality. Details regarding transistors in the MPS Accused Products are in the possession of the Defendant and are expected to be obtained through discovery. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
3. The VLSI semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 4.
4. The VLSI semiconductor device of claim 1, wherein the first active region and second active region contain digital logic formed by one of either p-channel and n-channel devices.	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 5; Exhibit A-2, Claim 4. Upon information and belief, the first and second active regions contain digital logic as claimed. *See* above at Claim 1, Element 6.
5. The VLSI semiconductor device of claim 1, wherein the	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 6.

Exhibit A-3 to Greenthread's Complaint

U.S. Patent No. 11,121,222	Accused Products
first active region and second active region contain either p-channel or n-channel devices in n−wells or p−wells, respectively, and each well has at least one graded dopant.	
6. The VLSI semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 7.
7. The VLSI semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 8.
8. The VLSI semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Elements 1-3.
9. The VLSI semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The MPS Accused Products meet this limitation. *See* Exhibit A-2, Claim 9.
13. The VLSI semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.	The MPS Accused Products meet this limitation. *See* Exhibit A-2, Claim 13. Upon information and belief, the transistors which can be formed in the first and second active regions are CMOS digital logic transistors as claimed. *See* above at Claim 1, Element 6.

Exhibit A-3 to Greenthread's Complaint

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15. The VLSI semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.	The MPS Accused Products meet this limitation. *See* Exhibit A-2, Claim 15.
16. The VLSI semiconductor device of claim 1, wherein the device is a flash memory.	The MPS Accused Products meet this limitation. *See* Exhibit A-2, Claim 16.
17. The VLSI semiconductor device of claim 1, wherein the device comprises digital logic and capacitors.	The MPS Accused Products meet this limitation. Upon information and belief, the semiconductor device comprises digital logic and capacitors. *See* above at Claim 1, Element 6 (discussion regarding digital logic). Details regarding digital logic and capacitors in the MPS Accused Products are in the possession of the Defendant and are expected to be obtained through discovery.
20. The VLSI semiconductor device of claim 1, wherein each of the first and second active regions are in the lateral or vertical direction.	The MPS Accused Products meet this limitation. As shown by SEM imaging (*see* Exhibit A-1, Claim 1, Elements 1-3), each of the first and second active regions are in the lateral or vertical direction.
[Claim 21, Preamble] A VLSI semiconductor device, comprising:	To the extent the preamble is a limitation, the MPS Accused Products include a semiconductor device. *See* above at Claim 1, Preamble.
[Claim 21, Element 1] a substrate of a first doping type at a first doping level having a surface;	The MPS Accused Products meet this limitation. *See* above at Claim 1, Element 1.
[Claim 21, Element 2] a first active region disposed adjacent the surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 9, Element 2.
[Claim 21, Element 3] a second active region separate from the	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 9, Element 3.

Exhibit A-3 to Greenthread's Complaint

U.S. Patent No. 11,121,222	Accused Products
first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	
[Claim 21, Element 4] transistors formed in at least one of the first active region or second active region;	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 4.
[Claim 21, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where there are no active regions; and	The MPS Accused Products meet this limitation. *See* above at Claim 1, Element 5. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 21, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface to the area of the substrate where there are no active regions, and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof.	The MPS Accused Products meet this limitation. *See* Exhibit A-2, Claim 1, Element 6. As shown by SCM/sMIM analysis (*see* Exhibit A-1, Claim 1, Element 1), the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof. For example, the quasilinear nature of the concentration is shown in the SCM/sMIM graph discussed at Exhibit A-1, Claim 1, Element 5. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
24. The VLSI semiconductor device of claim 21, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 4.
25. The VLSI semiconductor device of claim 21, wherein the	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 5.

Exhibit A-3 to Greenthread's Complaint

U.S. Patent No. 11,121,222	Accused Products
first active region and second active region contain at least one of either p-channel and n-channel devices.	
26. The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain either p-channel or n-channel devices in n−wells or p−wells, respectively, and each well has at least one graded dopant.	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 6.
27. The VLSI semiconductor device of claim 21, wherein the first active region and second active region are each separated by at least one isolation region.	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 7.
28. The VLSI semiconductor device of claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The MPS Accused Products meet this limitation. *See* Exhibit A-2, Claim 9.
32. The VLSI semiconductor device of claim 21, wherein the graded dopant is fabricated with an ion implantation process.	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 8.
33. The VLSI semiconductor device of claim 21, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device.	The MPS Accused Products meet this limitation. *See* Exhibit A-2, Claim 15.

Exhibit A-3 to Greenthread's Complaint

U.S. Patent No. 11,121,222	Accused Products
34. The VLSI semiconductor device of claim 21, wherein the device is a flash memory.	The MPS Accused Products meet this limitation. *See* Exhibit A-2, Claim 16.
[Claim 39, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the MPS Accused Products include a semiconductor device. *See* Exhibit A-1, Claim 1, Preamble.
[Claim 39, Element 1] a substrate of a first doping type at a first doping level;	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 1.
[Claim 39, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 2.
[Claim 39, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 3.
[Claim 39, Element 4] transistors formed in at least one of the first active region or second active region; and	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 4.
[Claim 39, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first or second active region to at least	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 5; *see* above at Claim 21, Element 5. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

Exhibit A-3 to Greenthread's Complaint

U.S. Patent No. 11,121,222	Accused Products
one substrate area where there is no active region.	
40. The semiconductor device of claim 39 further comprising at least one well region adjacent to the first or second active region and containing at least one graded dopant region, the graded dopant region to aid carrier movement from any region in the well to the substrate area where there is no well.	The MPS Accused Products meet this limitation. *See* Exhibit A-2, Claim 1, Element 6. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 41, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the MPS Accused Products include a semiconductor device. *See* above at Claim 39, Preamble.
[Claim 41, Element 1] a substrate of a first doping type at a first doping level;	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 1.
[Claim 41, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The MPS Accused Products meet this limitation. *See* above at Claim 39, Element 2.
[Claim 41, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The MPS Accused Products meet this limitation. *See* above at Claim 39, Element 3.
[Claim 41, Element 4] transistors formed in at least one of the first active region or second active region; and	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 4.

Exhibit A-3 to Greenthread's Complaint

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[Claim 41, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant acceptor concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.	The MPS Accused Products meet this limitation. *See* above at Claim 1, Element 5. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 42, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the MPS Accused Products include a semiconductor device. *See* above at Claim 39, Preamble.
[Claim 42, Element 1] a substrate of a first doping type at a first doping level;	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 1.
[Claim 42, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The MPS Accused Products meet this limitation. *See* above at Claim 39, Element 2.
[Claim 42, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The MPS Accused Products meet this limitation. *See* above at Claim 39, Element 3.
[Claim 42, Element 4] transistors formed in at least one of the first active region or second active region; and	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 4.
[Claim 42, Element 5] at least a portion of at least one of the first and second active regions having	The MPS Accused Products meet this limitation. SCM/sMIM analysis (*see* Exhibit A-1, Claim 1, Element 5) reveals at least one graded dopant acceptor concentration (e.g., concentration in n-well) as claimed. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5

Exhibit A-3 to Greenthread's Complaint

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at least one graded donor dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.	electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 44, Preamble] A CMOS Semiconductor device comprising:	To the extent the preamble is a limitation, the MPS Accused Products include a CMOS Semiconductor device. *See* Exhibit A-1, Claim 1, Preamble; Exhibit A-1, Claim 18.
[Claim 44, Element 1]: a surface layer;	The MPS Accused Products meet this limitation. *See* above at Claim 21, Element 1.
[Claim 44, Element 2] a substrate;	The MPS Accused Products meet this limitation. *See* above at Claim 44, Element 1.
[Claim 44, Element 3] an active region including a source and a drain, disposed on one surface of the surface layer;	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 2 (discussion of active region); Exhibit A-1, Claim 18 (discussion of source and drain).
[Claim 44, Element 4] a single drift layer disposed between the other surface of the surface layer and the substrate, the drift layer having a graded concentration of dopants extending between the surface layer and the substrate, the drift layer further having a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions; and	The MPS Accused Products meet this limitation. *See* above at Claim 21, Element 5. Upon information and belief, the drift layer has a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions as claimed, as a result of the above-discussed graded concentration of dopants. Details regarding electric field characteristics are in the possession of the Defendant and are expected to be obtained through discovery. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

Exhibit A-3 to Greenthread's Complaint

U.S. Patent No. 11,121,222	Accused Products
[Claim 44, Element 5] at least one well region disposed in the single drift layer, the well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions.	The MPS Accused Products meet this limitation. *See* above at Claim 21, Element 6. The well region (discussed above for Claim 21, Element 6) has a graded concentration of dopants. Upon information and belief, the well region is disposed in the single drift layer, and it has a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions as claimed, as a result of the well region's graded concentration of dopants. Details regarding electric field characteristics are in the possession of the Defendant and are expected to be obtained through discovery. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

Exhibit A-4 to Greenthread's Complaint

U.S. Patent No. 8,421,195	Accused Products
[Claim 1, Preamble] A CMOS Semiconductor device comprising:	To the extent the preamble is a limitation, the MPS Accused Products include a CMOS semiconductor device. The MPS Semiconductor 86905 Intelli-Phase Solution with integrated HS/LS-FETs and Driver ("86905") discussed for claim 1 of Exhibit A-3 is a semiconductor device (*see* Exhibit A-1, Claim 1, Preamble and Exhibit A-3, Claim 44, Preamble) with transistors, and is a CMOS semiconductor device upon information and belief. This chart includes exemplary information regarding a representative example of the MPS Accused Products, the MPS 86905. The MPS 86905 is representative of the MPS Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other MPS Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '195 patent (and the other asserted patents). For example, the other MPS Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '195 patent (and the other asserted patents). Similarly, the other MPS Accused Products (including MPS Accused Products) would have been designed in a similar manner as the MPS 86905 for purposes of this claim chart because to achieve such performance enhancements (e.g., on and off switching times). Therefore, upon information and belief the other MPS Accused Products contain similar features as the MPS 86905 transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other MPS Accused Products contain similar features as the MPS 86905, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1] a surface layer;	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 44, Element 1.
[Claim 1, Element 2] a substrate;	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 44, Element 2.
[Claim 1, Element 3] an active region including a source and a drain, disposed on one surface of said surface layer;	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 44, Element 3.
[Claim 1, Element 4] a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate, said drift layer further having a first static unidirectional electric drift field to aid the movement of minority	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 44, Element 4. Upon information and belief, the drift layer (*see* Exhibit A-3, Claim 44, Element 4) has a first static unidirectional electric drift field to aid the movement of minority carriers from the surface layer to the substrate, as claimed. Details regarding electric field characteristics are in the possession of the Defendant and are expected to be obtained through discovery. *See also* SCM/sMIM analysis reproduced at Exhibit A-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/SMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

Exhibit A-4 to Greenthread's Complaint

U.S. Patent No. 8,421,195	Accused Products
carriers from said surface layer to said substrate; and	
[Claim 1, Element 5] at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 44, Element 5. Upon information and belief, the well region has a second static unidirectional electric drift field to aid the movement of minority carriers from the surface layer to the substrate, as claimed. Details regarding electric field characteristics are in the possession of the Defendant and are expected to be obtained through discovery. *See also* SCM/SMIM analysis reproduced at Exhibit A-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/SMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
2. The CMOS Semiconductor device of claim 1, wherein the said drift layer is a deeply-implanted layer.	The MPS Accused Products meet this limitation. Upon information and belief, the drift layer is a deeply-implanted layer.
3. The CMOS Semiconductor device of claim 1, wherein said drift layer is an epitaxial layer.	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 4; Exhibit A-3, Claim 44, Element 4. Upon information and belief, the drift layer is grown above the substrate and is an epitaxial layer.
5. The CMOS Semiconductor device of claim 1, wherein said graded concentration follows a quasi-linear gradient.	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Elements 1, 5.
6. The CMOS Semiconductor device of claim 1, wherein said graded concentration follows an exponential gradient.	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Elements 1, 5.

Exhibit A-5 to Greenthread's Complaint

U.S. Patent No. 9,190,502	Accused Products
[Claim 7, Preamble] A semiconductor device comprising:	To the extent the preamble is a limitation, the MPS Accused Products include a semiconductor device. The MPS Semiconductor 86905 Intelli-Phase Solution with integrated HS/LS-FETs and Driver ("86905") discussed for claim 1 of Exhibit A-1 is a semiconductor device (*see* Exhibit A-1, Claim 1, Preamble) with transistors, and is a semiconductor device upon information and belief. Details regarding transistor count are in the possession of the Defendant and are expected to be obtained through discovery. This chart includes exemplary information regarding a representative example of the MPS Accused Products, the MPS 86905. The MPS 86905 is representative of the MPS Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other MPS Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '502 patent (and the other asserted patents). For example, the other MPS Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '502 patent (and the other asserted patents). Similarly, the other MPS Accused Products (including MPS Accused Products) would have been designed in a similar manner as the MPS 86905 for purposes of this claim chart because to achieve such performance enhancements (e.g., on and off switching times). Therefore, upon information and belief the other MPS Accused Products contain similar features as the MPS 86905 transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other MPS Accused Products contain similar features as the MPS 86905, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 7, Element 1] a surface layer;	The MPS Accused Products meet this limitation. *See* Exhibit A-4, Claim 1, Element 1.
[Claim 7, Element 2] a substrate;	The MPS Accused Products meet this limitation. *See* Exhibit A-4, Claim 1, Element 2.
[Claim 7, Element 3] an active region including a source and a drain, disposed on one surface of said surface layer;	The MPS Accused Products meet this limitation. *See* Exhibit A-4, Claim 1, Element 3.
[Claim 7, Element 4] a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants generating a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate;	The MPS Accused Products meet this limitation. *See* Exhibit A-4, Claim 1, Element 4. The graded concentration of dopants observed via SCM/sMIM analysis (*see* Exhibit A-1, Claim 1, Elements 1, 5) generates a first static unidirectional electric drift field to aid the movement of minority carriers, as claimed. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

Exhibit A-5 to Greenthread's Complaint

U.S. Patent No. 9,190,502	Accused Products
[Claim 7, Element 5] and at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants generating a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.	The MPS Accused Products meet this limitation. *See* Exhibit A-4, Claim 1, Element 5. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
8. The semiconductor device of claim 7 wherein said first and second static unidirectional electric fields are adapted to respective grading of dopants to aid movements of carriers in respective active regions.	The MPS Accused Products meet this limitation. Upon information and belief, the first and second static unidirectional electric fields are adapted to respective grading of dopants to aid movements of carriers in respective active regions. Details regarding the electric fields and active regions are in the possession of the Defendant and are expected to be obtained through discovery. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

Exhibit A-6 to Greenthread's Complaint

U.S. Patent No. 11,316,014	Accused Products
[Claim 1, Preamble] An electronic system, the system comprising:	To the extent the preamble is a limitation, the MPS Accused Products include an electronic system. *See* Exhibit A-1, Claim 1, Preamble; Exhibit A-4, Claim 1, Preamble. Each MPS Accused Product is an electronic system. This chart includes exemplary information regarding a representative example of the MPS Accused Products, the MPS 86905. The MPS 86905 is representative of the MPS Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other MPS Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '014 patent (and the other asserted patents). For example, the other MPS Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '014 patent (and the other asserted patents). Similarly, the other MPS Accused Products (including MPS Accused Products) would have been designed in a similar manner as the MPS 86905 for purposes of this claim chart because to achieve such performance enhancements (e.g., on and off switching times). Therefore, upon information and belief the other MPS Accused Products contain similar features as the MPS 86905 transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other MPS Accused Products contain similar features as the MPS 86905, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1a] at least one semiconductor device, the at least one semiconductor device including:	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Preamble.
[Claim 1, Element 1b] a substrate of a first doping type at a first doping level having a surface;	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 1, Element 1.
[Claim 1, Element 1c] a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 1, Element 2; Exhibit A-1, Claim 9, Element 2.
[Claim 1, Element 1d] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 1, Element 3; Exhibit A-1, Claim 9, Element 3.
[Claim 1, Element 1e] transistors formed in at least one of the first active region or second active region;	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 1, Element 4.

Exhibit A-6 to Greenthread's Complaint

U.S. Patent No. 11,316,014	Accused Products
[Claim 1, Element 1f] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 1, Element 5. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 1, Element 1g] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the semiconductor device.	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 1, Element 6; Exhibit A-3, Claim 21, Element *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
3. The system of Claim 1, wherein the substrate of the at least one semiconductor device has epitaxial silicon on top of a nonepitaxial substrate.	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 3.
4. The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device contain digital logic formed by one of either p-channel and n-channel devices.	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 4.
5. The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 5.
6. The system of Claim 1, wherein the first active region and second active region of the at least one	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 6.

Exhibit A-6 to Greenthread's Complaint

U.S. Patent No. 11,316,014	Accused Products
semiconductor device are each separated by at least one isolation region.	
7. The system of Claim 1, wherein the graded dopant is fabricated with an ion implantation process.	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 7.
8. The system of Claim 1, wherein the first and second active regions of the at least one semiconductor device are formed adjacent the first surface of the substrate of the at least one semiconductor device.	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 8.
9. The system of Claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one semiconductor device are either p-type or n-type.	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 9.
13. The system of claim 1, wherein the transistors which can be formed in the first and second active regions of the at least one semiconductor device are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 13.
15. The system of Claim 1, wherein the at least one semiconductor device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 15.
16. The system of Claim 1, wherein the at least one semiconductor device is a flash memory.	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 16.
17. The system of Claim 1, wherein the at least one semiconductor device comprises digital logic and capacitors.	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 17.
20. The system of Claim 1, wherein each of the first and second active regions of the at least one	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 20.

Exhibit A-6 to Greenthread's Complaint

U.S. Patent No. 11,316,014	Accused Products
semiconductor device are in the lateral or vertical direction.	
[Claim 21, Preamble] An electronic system, the system comprising:	To the extent the preamble is a limitation, the MPS Accused Products include an electronic system. *See* above at Claim 1, Preamble.
[Claim 21, Element 1a] at least one semiconductor device, the at least one semiconductor device including:	The MPS Accused Products meet this limitation. *See* above at Claim 1, Element 1a.
[Claim 21, Element 1b] a substrate of a first doping type at a first doping level having a surface;	The MPS Accused Products meet this limitation. *See* above at Claim 1, Element 1b.
[Claim 21, Element 1c] a first active region disposed adjacent the surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;	The MPS Accused Products meet this limitation. *See* above at Claim 1, Element 1c; Exhibit A-1, Claim 9, Element 2.
[Claim 21, Element 1d] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	The MPS Accused Products meet this limitation. *See* above at Claim 1, Element 1d; Exhibit A-1, Claim 9, Element 3.
[Claim 21, Element 1e] transistors formed in at least one of the first active region or second active region;	The MPS Accused Products meet this limitation. *See* above at Claim 1, Element 1e.
[Claim 21, Element 1f] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where there are no active regions; and	The MPS Accused Products meet this limitation. *See* above at Claim 1, Element 1f; Exhibit A-1, Claim 9, Element 5. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 21, Element 1g] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier thereof movement from the surface	The MPS Accused Products meet this limitation. *See* above at Claim 1, Element 1g; Exhibit A-3, Claim 21, Element 6. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

Exhibit A-6 to Greenthread's Complaint

U.S. Patent No. 11,316,014	Accused Products
to the area of the substrate where there are no active regions, and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof.	
23. The system of Claim 21, wherein the substrate of the at least one semiconductor device is a p-type substrate.	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 23.
24. The system of Claim 21, wherein the substrate of the at least one semiconductor device has epitaxial silicon on top of a nonepitaxial substrate.	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 24.
25. The system of Claim 21, wherein the first active region and second active region of the at least one semiconductor device contain at least one of either p-channel and n-channel devices.	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 25.
26. The system of Claim 21, wherein the first active region and second active region of the at least one semiconductor device contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 26.
27. The system of Claim 21, wherein the first active region and second active region of the at least one semiconductor device are each separated by at least one isolation region.	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 27.
28. The system of Claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 28.

Exhibit A-6 to Greenthread's Complaint

U.S. Patent No. 11,316,014	Accused Products
semiconductor device are either p-type or n-type.	

Tech Insights

techinsights.com

Monolithic Power Systems
MP86905
Intelli-Phase™ Solution with Integrated HS/LS-FETs and Driver

Power Essentials Summary

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PEF-2202-801

114309OODC

Published: April 28, 2022

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Overview

This a Power Essentials (PEF) summary document, provided as a companion deliverable for Power Essentials projects. The complete PEF deliverable includes this document, which provides a summary of observed device metrics and salient features, the summary is supported by the following unannotated image folders:

- Package optical photographs, package X-ray images, die photographs, optical photos of die feature image set
- Plan-view images of the device delayered to the gate level
- Exploratory cross-sectional scanning electron microscope (SEM) images of the device structure
- Detailed cross-sectional scanning capacitance microscopy (SCM) and scanning microwave impedance microscopy (sMIM-C) analysis of the dopant structures
- Detailed cross-sectional transmission electron microscope (TEM) images of the power device structure
- Metal and dielectric layer composition identification based on TEM-EDS results

The image set for a standard PEF project is derived from a beveled sample for SEM planar analysis, one plane of cross-sectioning for SEM structural analysis, a single TEM sample for the detailed structural analysis, and planar and cross-sectional SCM and sMIM analysis. Value added information, such as additional planes of cross-sectioning, may be included on a case-by-case basis.

The Power Essentials deliverable provides basic competitive benchmarking information and enables cost-effective tracking of multiple competitors' technology.

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Company Profile

- Monolithic Power Systems (MPS) is a global analog semiconductor company founded in 1997 by Michael Hsing and headquartered in Kirkland, Washington, U.S. The company provides semiconductor-based power electronics circuit for systems found in cloud computing, telecom infrastructures, automotive, industrial applications and consumer applications [1]. As of the end of December 2021, MPS reported an annual sales figure of $1.21 billion and had 2,209 employees in 2020.

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Device Summary

- This report presents a Power Essentials analysis of the MPS MP86905 silicon (Si)-based power management IC (PMIC). The MP86905 is a monolithic half-bridge with built-in internal power MOSFETs and gate drivers and is ideally suited for multi-phase buck regulators. It offers 50 A continuous output current over a wide 4.5 V to 16 V operating input range [2].
- The MP86905 comprises a single die with MP9502 die markings, which are encapsulated in a 23-pin flip-chip quad-flat-no-lead (FC-QFN) package with likely copper (Cu) bumping directly to the leadframe.
- The MP9502 die substrate is ~155 µm thick including the upper epitaxy layer and uses Bipolar-CMOS-DMOS (BCD) technology. It features a single layer of polysilicon in the analyzed regions, three aluminum (Al) metal layers, tungsten (W) contacts and vias, cobalt silicide (CoSi) at the source, drain, and polysilicon contact regions. The pre-metal dielectric (PMD) uses silicon oxide (SiO) layers, while the inter-metal dielectric (IMD) layers uses oxide as well. Isolation structures include shallow trench isolation (STI) in the logic region.
- One group of high side MOSFET (HSFET) array and two groups of low side MOSFET (LSFET) array are used on the die. The structure and dopants of the HS/LS FET arrays are analyzed. Dopant analysis in the HS/LS FET array region shows the use of a P-type substrate, an N-type buried layer (NBL), a N-drift/N-well layer and a P-well layer.
- The stepped-gate-oxide (SGO) is used in the LDMOS devices on this die. The use of SGO allows a reduction of on-resistance (Ron) compared with the conventional STI LDMOS [3].
- The HSFET is arranged in a one-dimensional (1D) array with a ~4.0 µm drain-to-drain pitch and ~0.66 µm total polysilicon gate length, while the LSFET is arranged with ~3.4 µm drain-to-drain pitch and ~0.60 µm total polysilicon gate length in total.
- In the logic region, the minimum observed gate length is 0.40 µm on a 0.86 µm contacted gate pitch, indicating the use of likely 0.18 µm process generation with relaxed feature dimensions.

Manufacturer	Monolithic Power Systems
Part number	MP86905
Foundry	Unknown
Type	PMIC
Date code	H39 (week 39 of 2017)
Package type	23-pin FC-QFN
Package markings	MPSH39 M86905 54U403
Package dimensions	3.97 mm × 3.97 mm × 0.88 mm (thick)
Die markings	MP9502 2013 <MPS logo>
Die size (whole die)	3.38 mm × 3.14 mm (10.61 mm²)
Die size (edge seal)	3.36 mm × 3.12 mm (10.48 mm²)
Minimum measured transistor gate length/pitch	0.40 µm/0.86 µm
Process generation	Likely 0.18 µm process generation with relaxed feature dimensions
Feature measured to determine process generation	Contacted gate pitch, use of CoSi contacts, STI isolation
Maximum voltage [2]	18 V

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Observed Critical Dimensions – CMOS/LDMOS

Feature	Material Composition	Dimension (µm)
Gate length	Polysilicon	0.40
Contacted gate pitch	–	0.86
SWS widths	SiO/SiN	15 nm/70 nm
Polysilicon thickness	Si	0.18
STI depth	SiO	0.36

CMOS

Feature	Material Composition	Dimension (µm)
Cell pitch	–	4.0/3.4 (HS/LS)
Channel length	–	~0.17
Polysilicon thickness	Si	0.18
Polysilicon width	Si	0.66/0.60 (HS/LS)
Gate dielectric thickness	SiO	8.5 nm
SWS widths	SiO/SiN	15 nm/70 nm
CESL thickness	SiN	33 nm
Gate and contact silicide depth	CoSi	≤ 30 nm
SGO thickness	SiO	40 nm
N^+ S/D depth	–	0.20
N-well/N-drift depth	–	1.2
P-well depth	–	2.1
P-body depth	–	1.3

Output Channel LDMOS

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Observed Critical Dimensions – Metals/Dielectrics

Layer	Material Composition	Thickness (µm)
Passivation	SiN/SiO	0.75/0.80
IMD 2	SiO	1.40 (planarized)
IMD 1	SiO	1.40 (planarized)
PMD (PMD 2, PMD 1)	SiO	0.40/0.20 (planarized)
M3	TiN/Al/TiN	0.06/0.84/0.05
M2	TiN/Al/TiN	0.06/0.45/0.05
M1	TiN/Al/TiN	0.06/0.45/0.05
Die (total)	–	161

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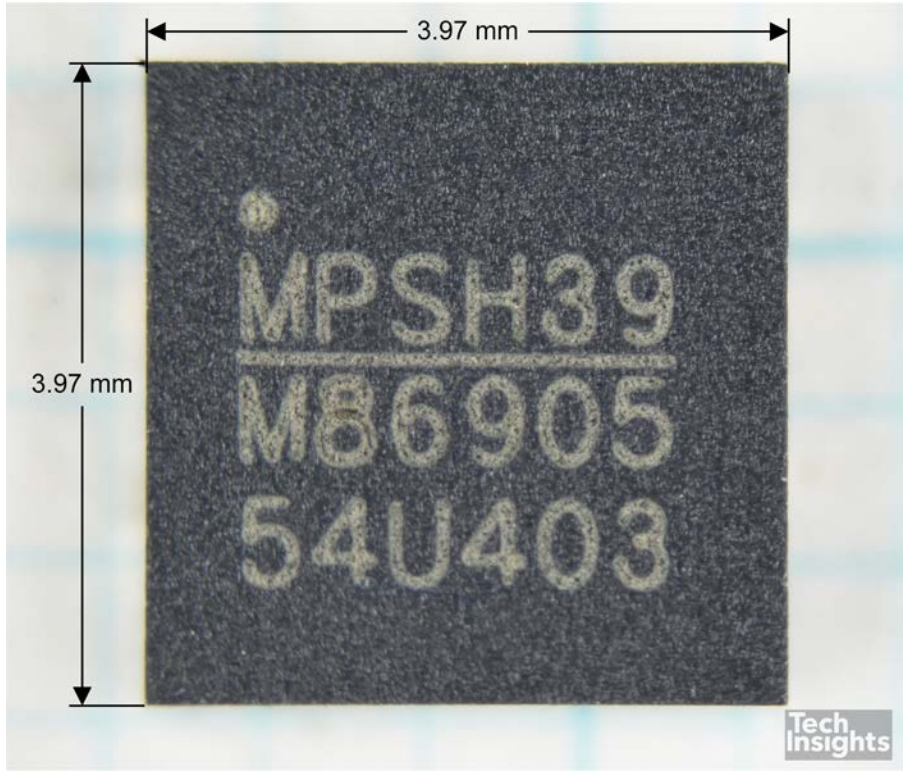
MP86905 Package Photographs

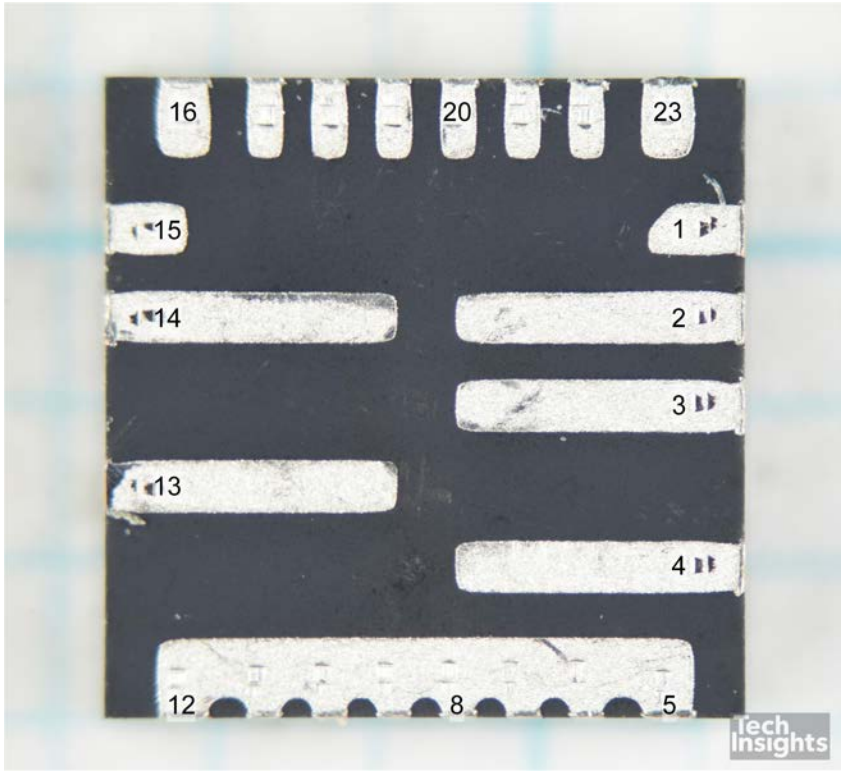
- Package markings include: MPSH39
  M86905
  54U403



MP86905GR-P_Pkg_Top_394747.png

Package – Top

- 23-pin FC-QFN page dimensions: 3.97 mm × 3.97 mm × 0.88 mm (thick)
- Detailed pin descriptions are presented on the next two pages.



MP86905GR-P_Pkg_Bot_394747.png

Package – Bottom

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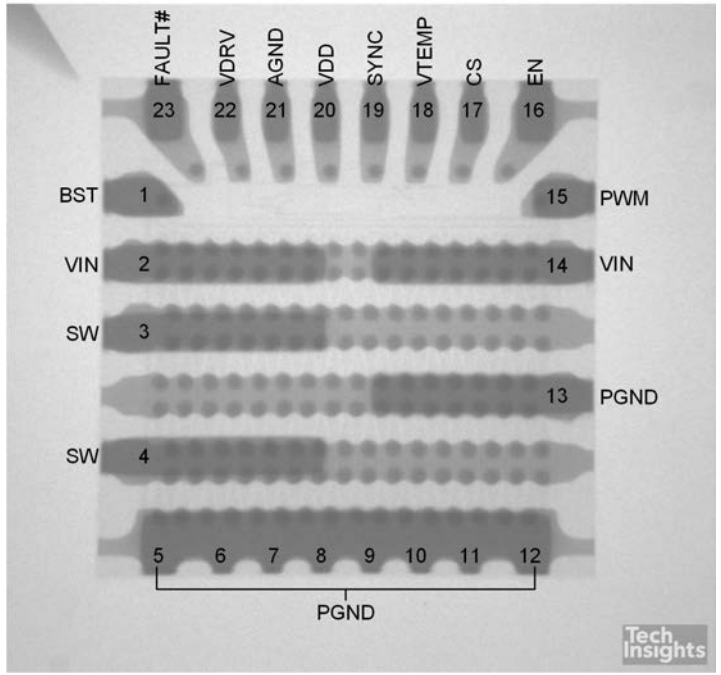
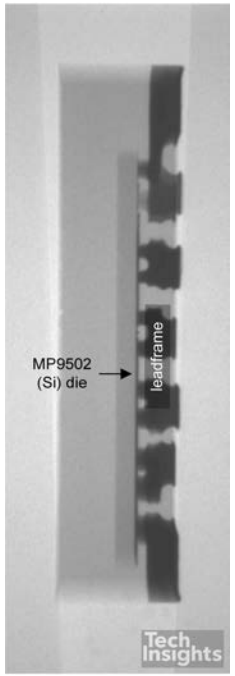
MP86905 Package X-Rays

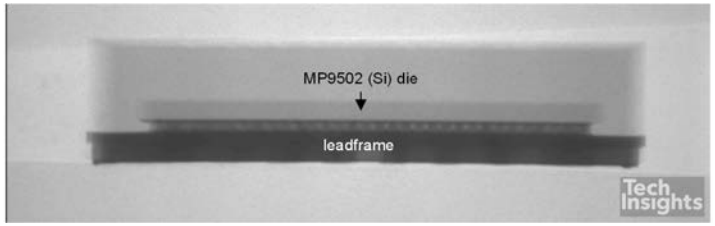
- Detailed pin descriptions are presented on the next page.



MP86905GR-P_XrayTop_394747.png



MP86905GR-P_XraySideB_394747.png



MP86905GR-P_XraySideA_394747.png

Package X-Rays

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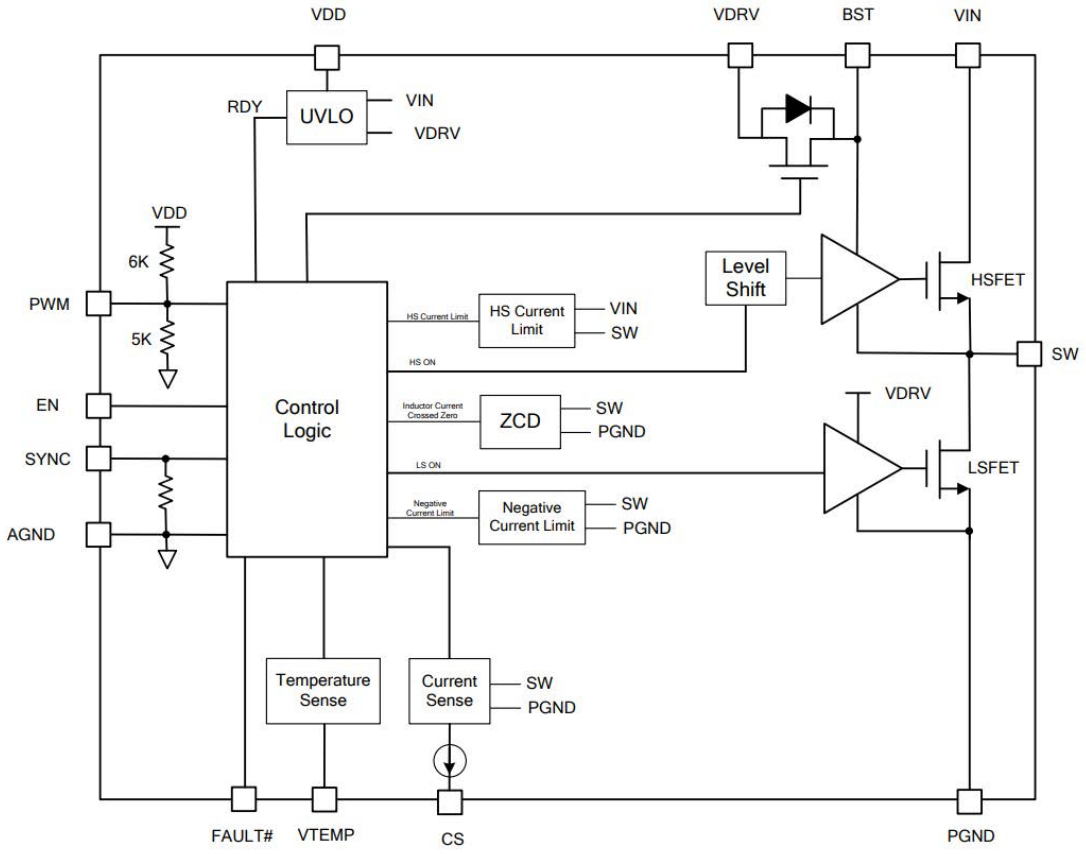
MP86905 Block Diagram with Pin Descriptions



Block Diagram [2]

Pin #	Name	Description
1	BST	**Bootstrap.** BST requires a 0.1µF to 1µF capacitor to drive the high-side power switch's gate above the supply voltage. Connect the capacitor between BST and SW to form a floating supply across the power switch driver.
2, 14	VIN	**Supply voltage.** Place C_{IN} close to the device to support the switching current and reduce voltage spikes at input.
3, 4	SW	**Phase node.**
5 - 13	PGND	**Power ground.**
15	PWM	**Pulse width modulation input.** Leave PWM floating or drive PWM to mid-state to enter diode emulation mode.
16	EN	**Enable.** Pull EN low to disable the device and place SW in a high impedance state.
17	CS	**Current sense output.**
18	VTEMP	**Junction temperature sense output.**
19	SYNC	**Diode emulation mode.** Pull SYNC low to enable diode emulation mode.
20	VDD	**Internal circuitry voltage.** Connect VDD to VDRV through a 2.2Ω resistor and decouple with a 1µF capacitor to AGND.
21	AGND	**Analog ground.** Connect AGND to PGND on the VDD capacitor.
22	VDRV	**Driver voltage.** Connect VDRV to a 3.3V supply and decouple with a 1µF to 4.7µF ceramic capacitor close to VDRV to PGND.
23	FAULT#	**Fault report.** FAULT# is an open drain, active low. FAULT# pulls low when SW short detection, HS current limit, or over-temperature is triggered. During a cycle-by-cycle high-side current limit event, FAULT# is kept high until the fourth cycle.

Pin Function Descriptions [2]

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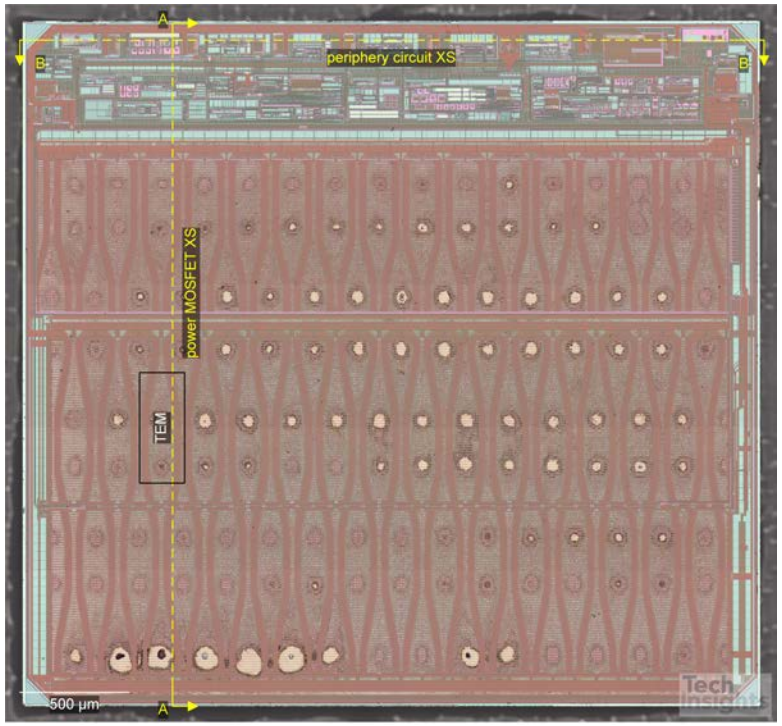
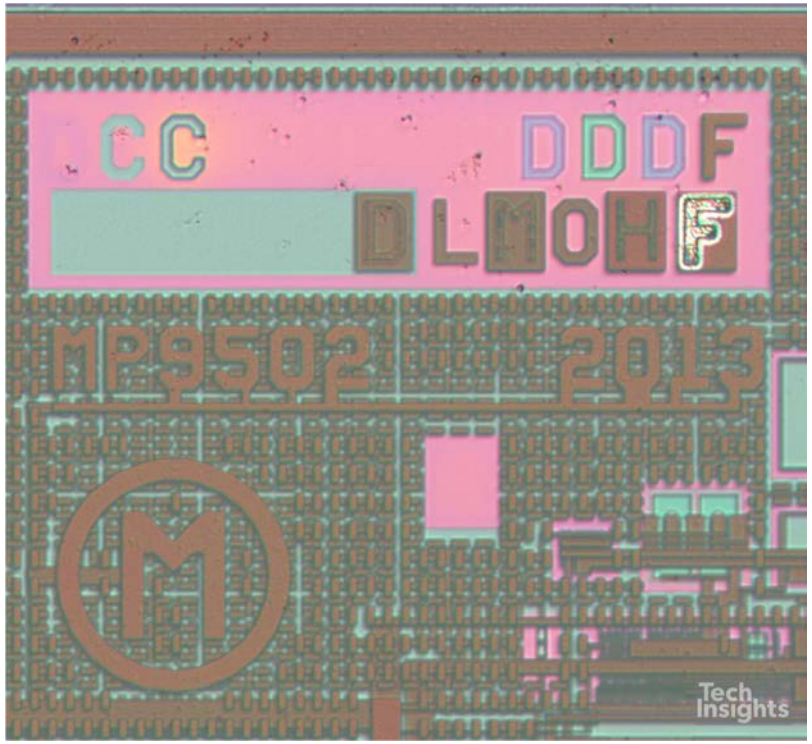
MP9502 Die Photograph and Die Markings

- Die size: 3.38 mm × 3.14 mm (10.61 mm²) (whole die)
  3.36 mm × 3.12 mm (10.48 mm²) (edge seal)
- The die SEM and SCM/sMIM-C cross-section line (A-A), TEM cross-section region, and an additional SEM cross-section line (B-B) are annotated.



M86908_MP9502_345783_Oriented.png

Die Photograph



M86908_MP9502_345783_DieMrk.png

Die Markings

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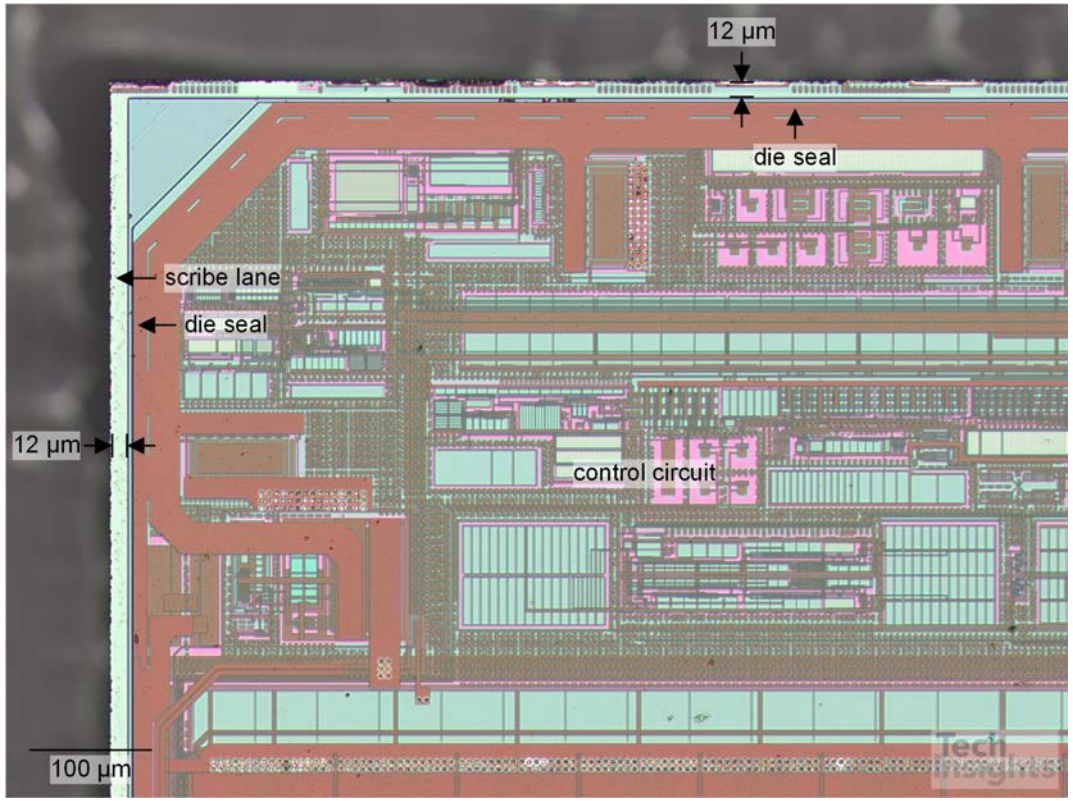
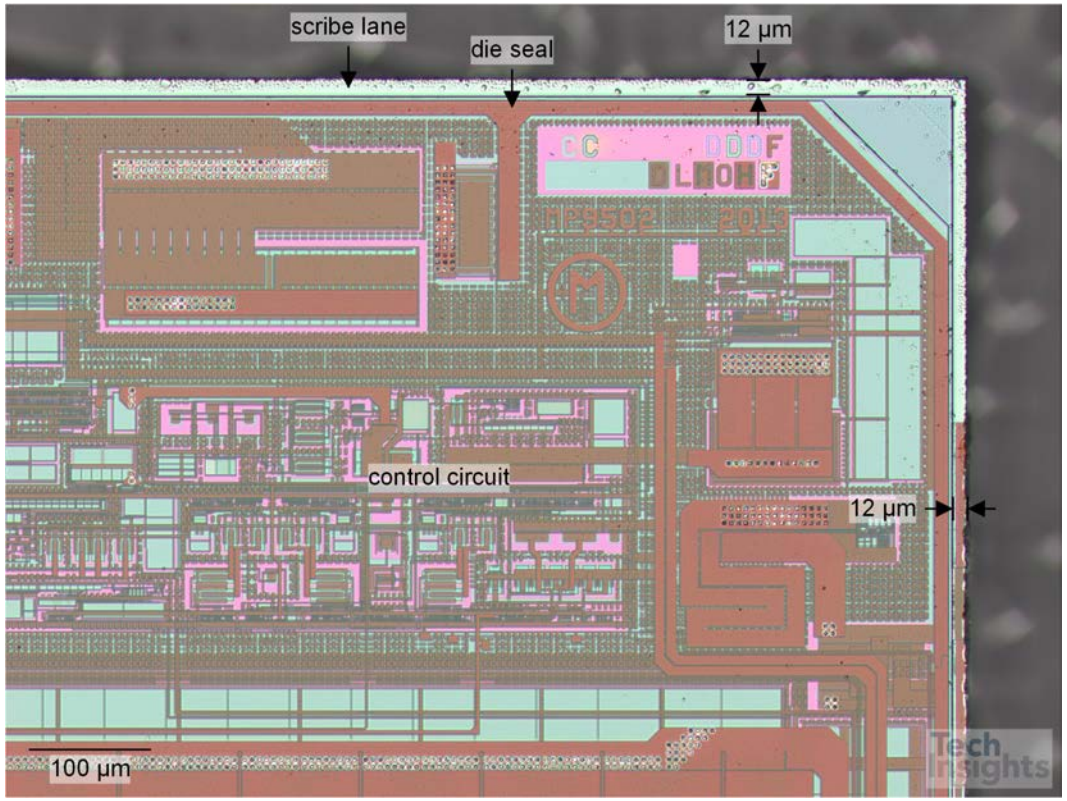
MP9502 Die Upper Corners

- The scribe lane measures ~12 µm wide all around the die.
- The control circuit is at the top portion of the die.



M86908_MP9502_345783_DieCornerA.png



M86908_MP9502_345783_DieCornerB.png

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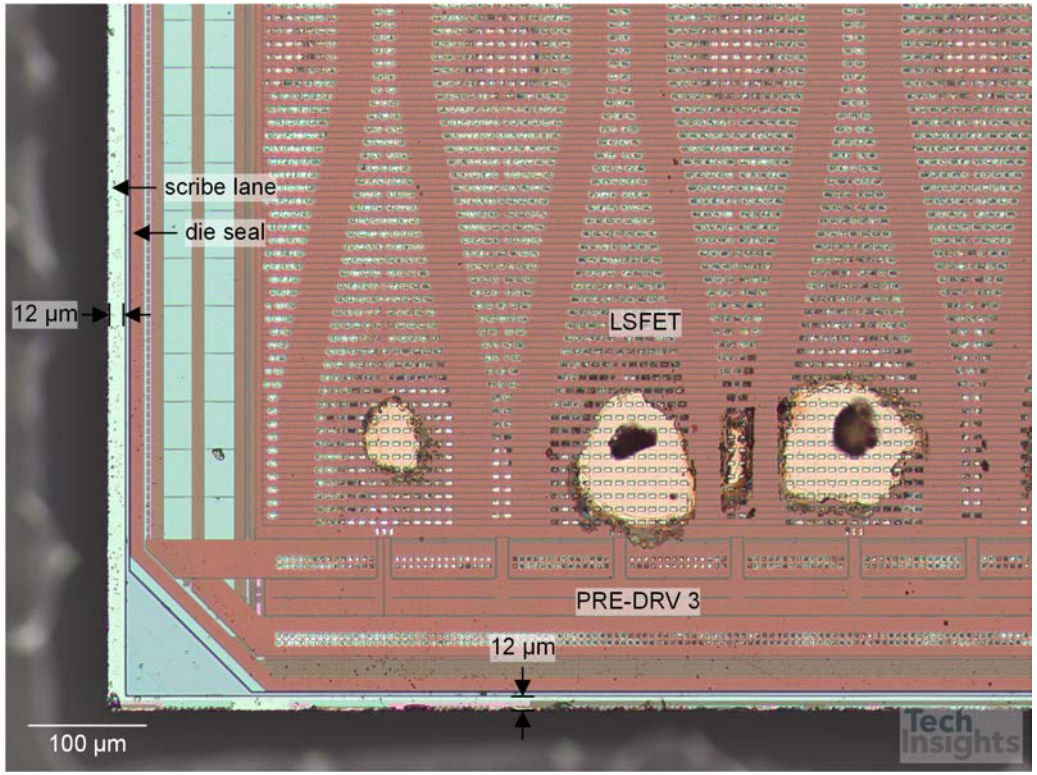
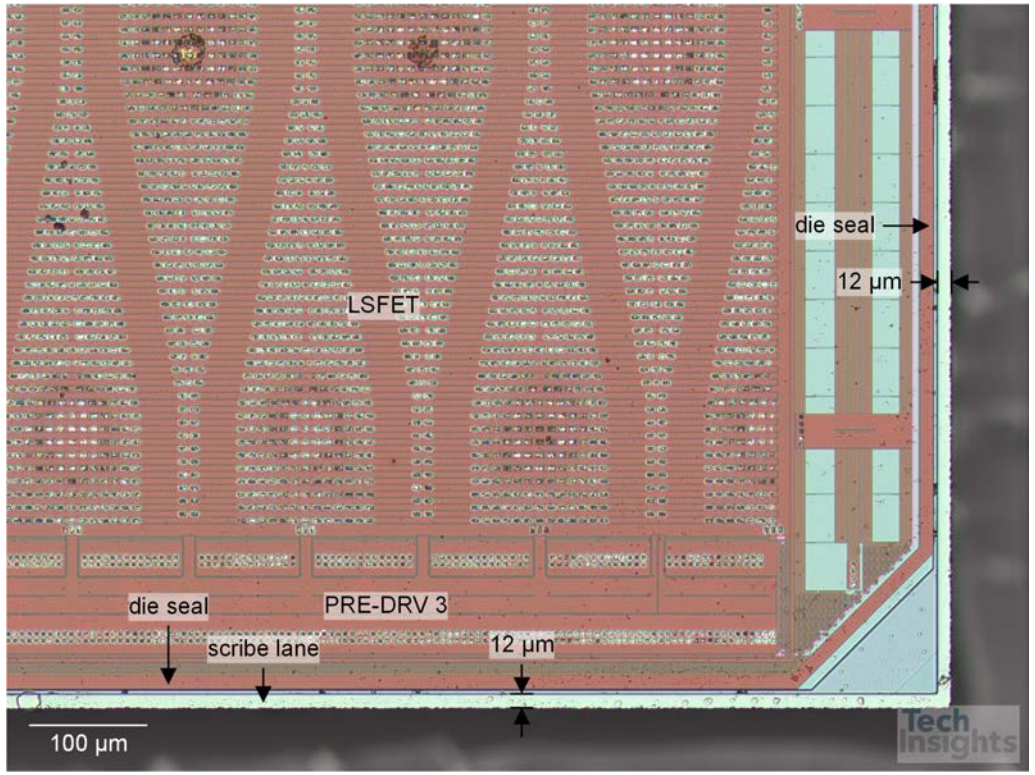
MP9502 Die Lower Corners

- The scribe lane measures ~12 µm wide all around the die.
- The low side MOSFET (LSFET) array and PRE-DRV 3 are at the bottom portion of the die.



M86908_MP9502_345783_DieCornerD.png



M86908_MP9502_345783_DieCornerC.png

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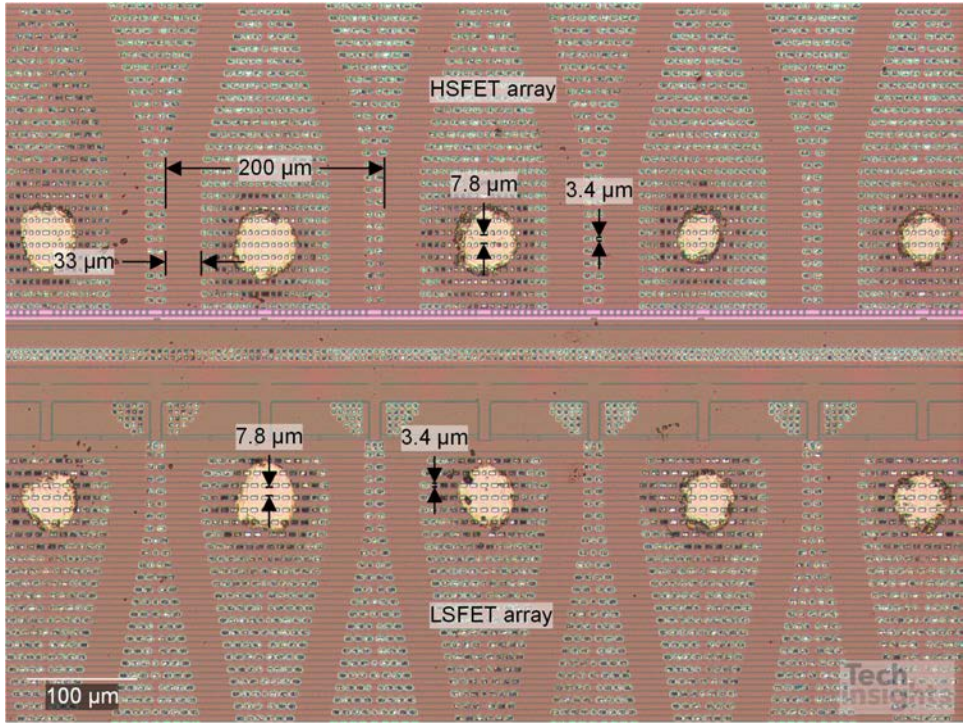
MP9502 MOSFET Die RDL Contacts

- Source/drain (S/D) groups of passivation openings are shown with the removed redistribution layer (RDL) contacts which are made through passivation openings.
- S/D groups of passivation openings have a spacing of 33 µm on a 200 µm pitch in the horizontal direction.
- S/D passivation openings have been placed horizontally with vertically minimal 7.8 µm spacing and 3.4 µm wide window.



M86908_MP9502_345783_BondPads.png

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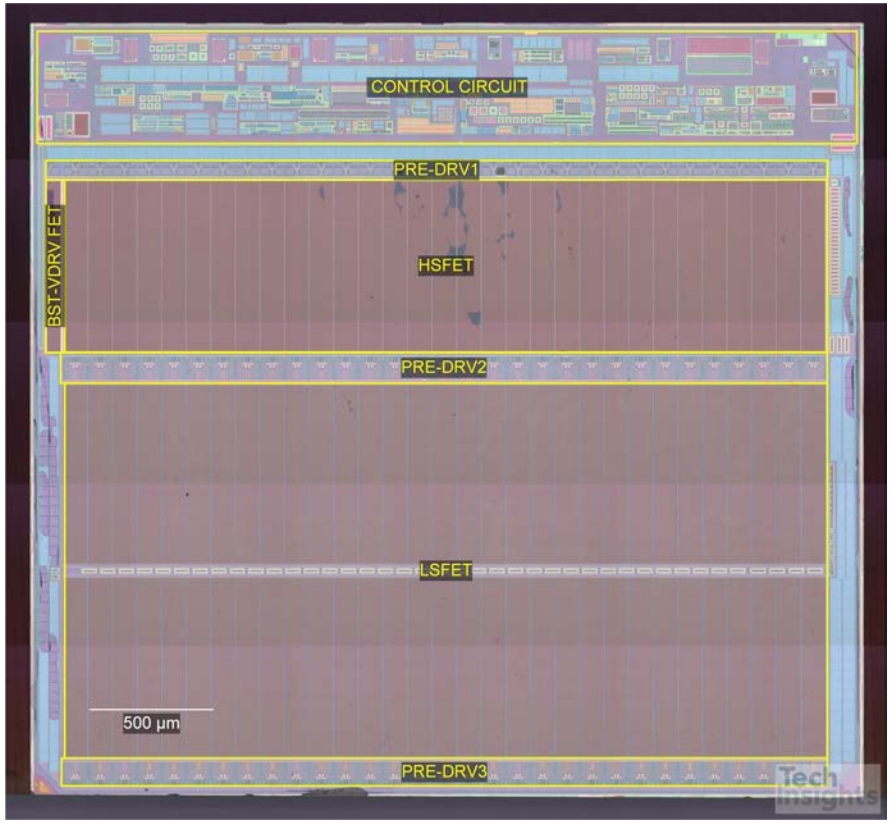
MP9502 Die Photograph at the Gate Layer

- The die was deprocessed to the polysilicon gate level.
- The die utilization is characterized in the table on the right.



MP86905GR-P_MP9502_394865_BPoly_Blocks.png

Functional Description	Length (mm)	Width (mm)	Area (mm^2)	Percentage of Die (%)
HSFET (High-side FET connected between VIN and SW pins)	0.70	3.10	2.18	20.8
LSFET (Low-side FET connected between SW and PGND pins)	1.53	3.10	4.73	45.1
PRE-DRV1 (Likely pre-drivers to the HSFET or LSFET)	0.08	3.18	0.25	2.4
PRE-DRV2 (Likely pre-drivers to the HSFET or LSFET)	0.12	3.12	0.39	3.7
PRE-DRV3 (Likely pre-drivers to the LSFET)	0.11	3.12	0.35	3.3
BST-VDRV FET (Likely a smaller version of FET connected between the BST pin and VDRV pin, this FET can also be used for temperature detection)	0.08	0.70	0.05	0.5
COTROL CIRCUIT (This analog control block consists of several analog circuits including, under-voltage lockout detection, over-temperature detection, over-voltage sensing and over-current sensing, bandgap, bias generator, current limiter and driving circuitry that drives the pre-drivers)	0.46	3.33	1.52	14.5
Total die utilization			9.47	90.3
Others (including capacitors that are not related to the circuit mentioned above and including small FETs on the right that looks like temperature detectors)	–		1.01	9.7
Total die	3.12	3.36	10.48	100.0

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General Structure Cross-Sectional Analysis

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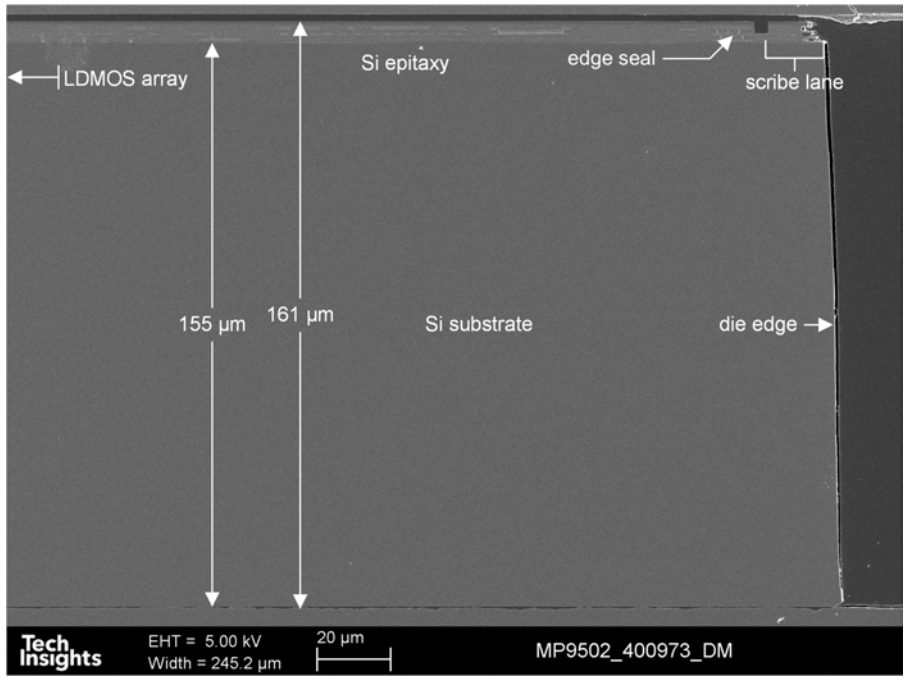
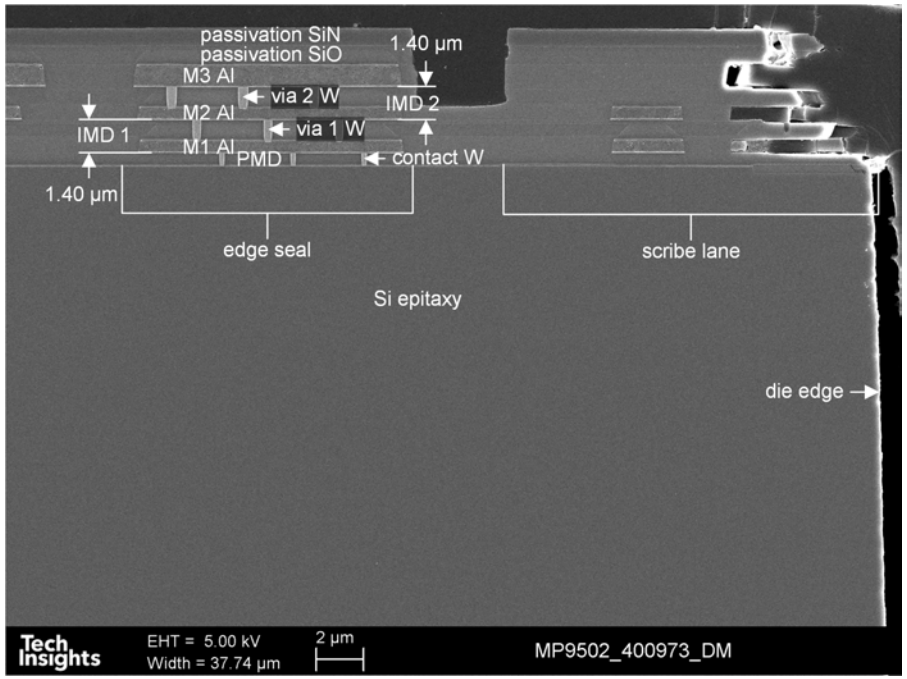
MP9502 Die Structural Overview

- The Si die substrate is ~155 µm thick including the upper epitaxy layer and ~161 µm thick in total.
- The die comprises three Al metallization layers with W vias and contacts.
- The crack stop at the die edge extends through the passivation into IMD 2.
- Both IMD 2 and IMD 1 are ~1.40 µm thick in the SEM sample.



Die Thickness_01_400973.png

Die Edge – SEM Cross-Section A-A



Die Edge_02_400973.png

Structural Overview at the Edge Seal – SEM Cross-Section A-A

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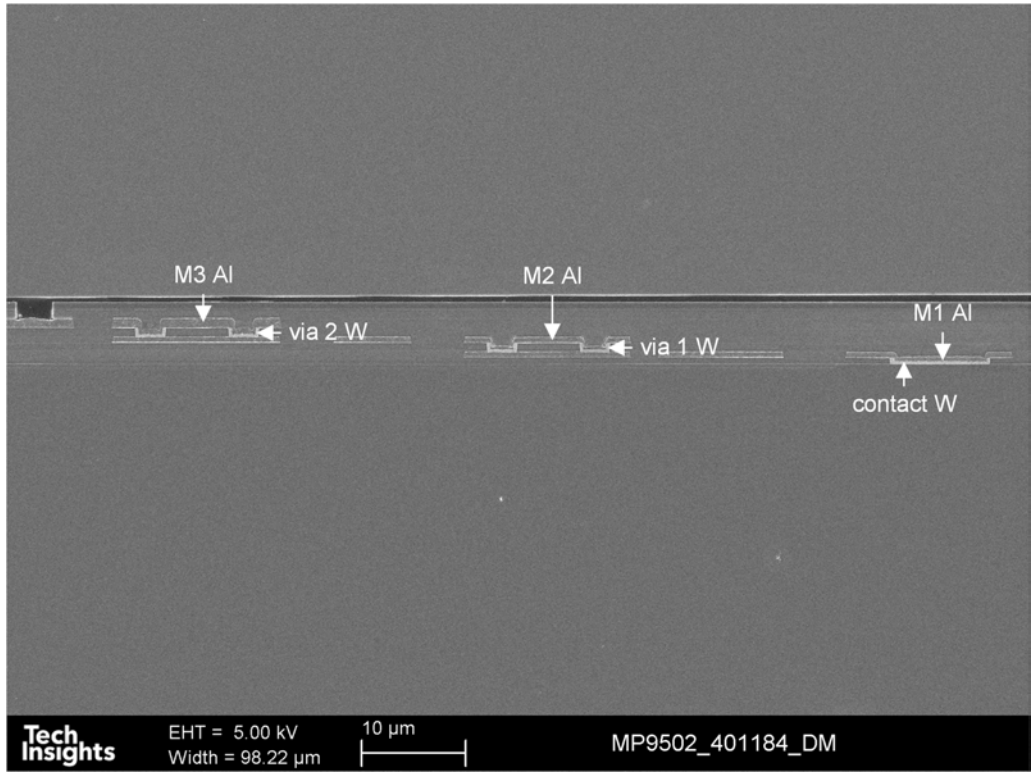
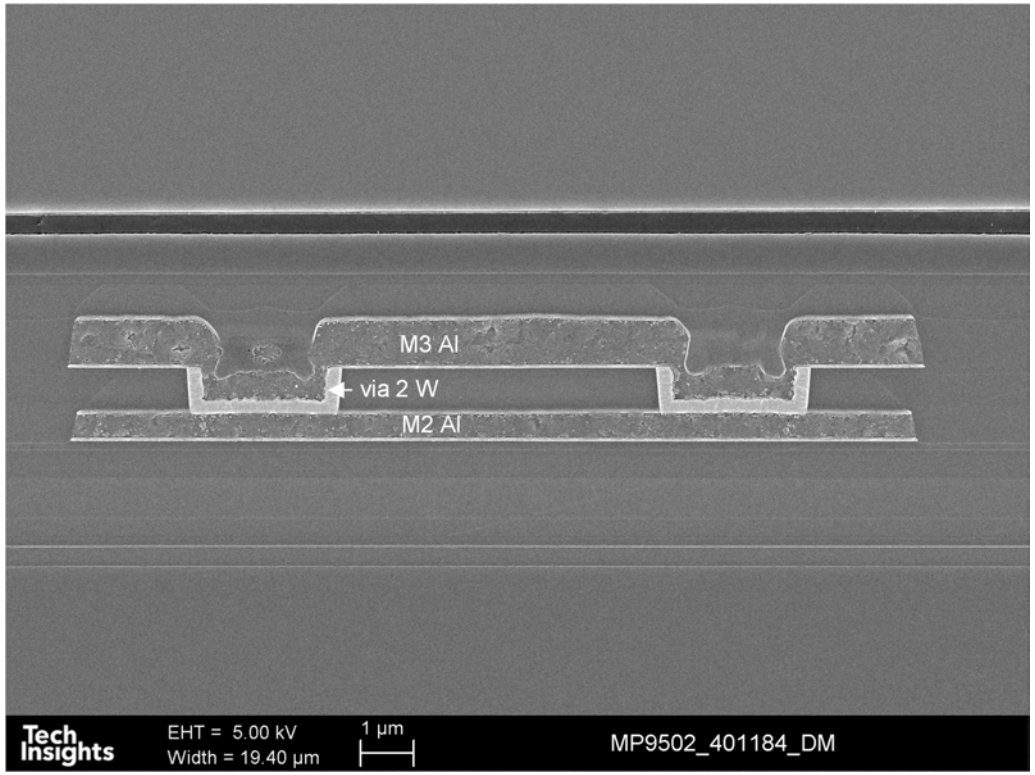
MP9502 Die Contact and Vias

- Wide via is formed with a conformal upper metal layer formed over the via trench lined with the via metallization, such as via 1 and via 2.



General Structure_43_401184.png

Wide Contact and Vias – SEM Cross-Section B-B



General Structure_42_401184.png

Wide Via 2 – SEM Cross-Section B-B

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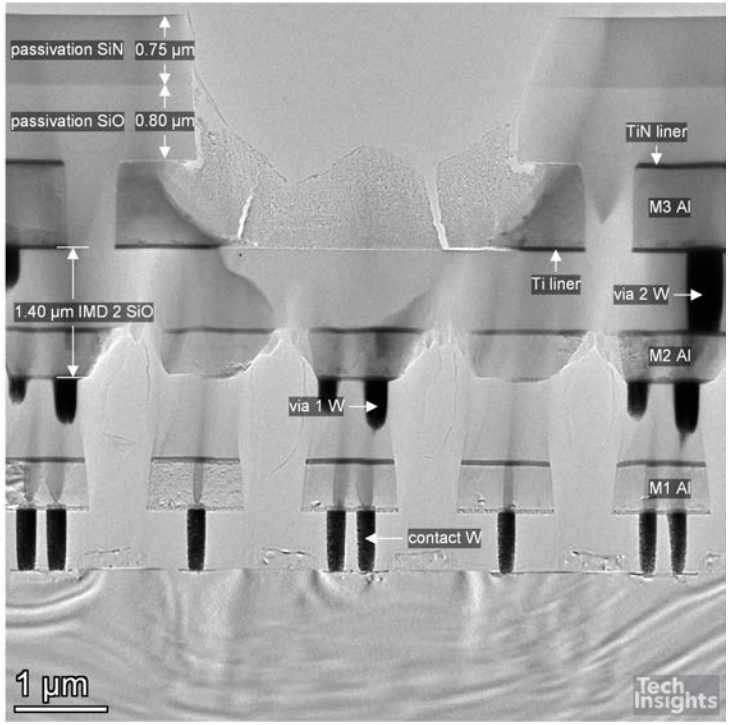
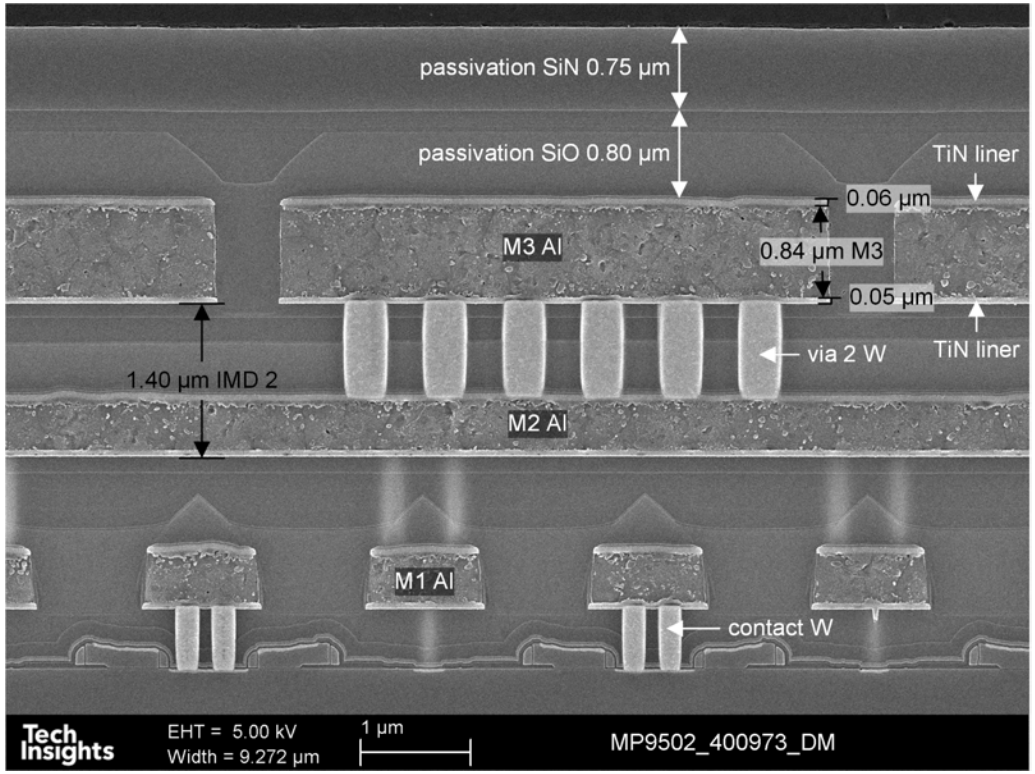
MP9502 Die Passivation, Metal 3, and IMD 2

- The passivation comprises an ~0.80 µm thick SiO and an ~0.75 µm thick SiN.
- Metal 3 comprises of an ~0.84 µm thick Al layer, with an ~0.05 µm thick bottom TiN liner, and ~0.06 µm thick top TiN liner.
- The IMD 2 layer comprises of an ~1.4 µm thick oxide.



20220329 1541 7000 x_400282.png

Passivation and Metal 3 – TEM Cross-Section



General Structure_40_400973.png

IMD 2 Details – SEM Cross-Section A-A

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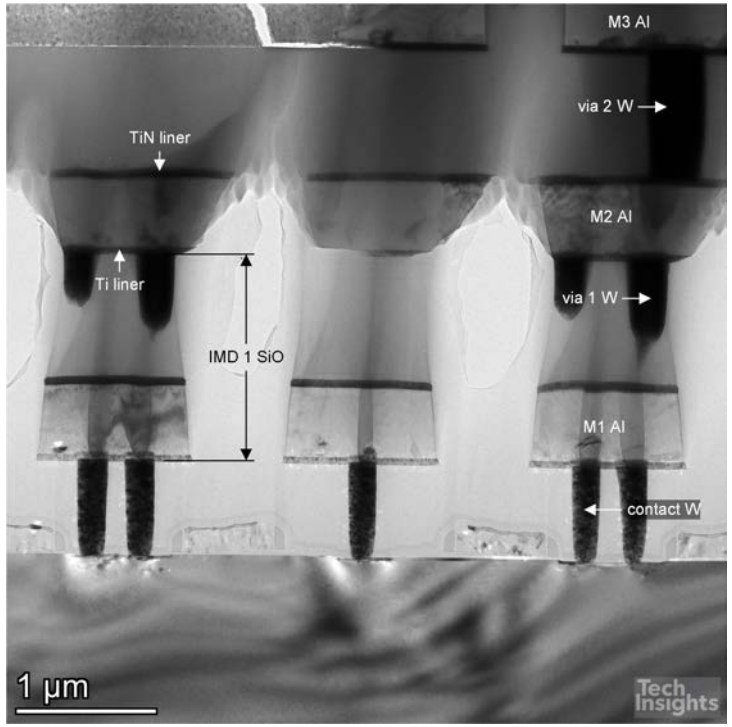
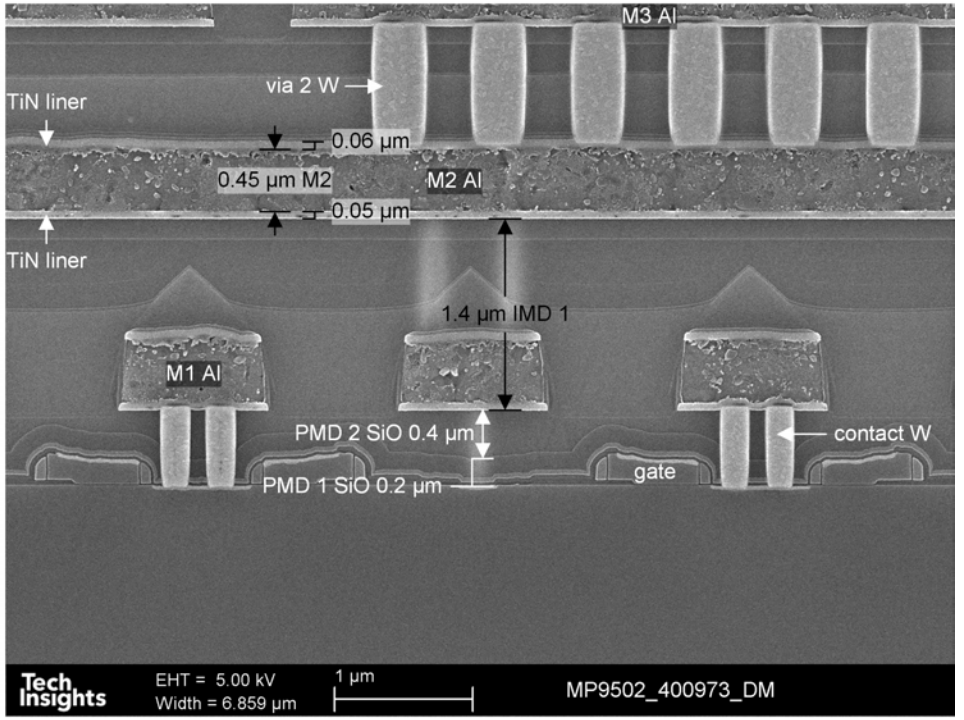
MP9502 Die Metal 2 and IMD 1

- Metal 2 comprises of an ~0.45 µm thick Al layer, with an ~0.05 µm thick bottom TiN liner and ~0.06 µm thick top TiN liner.
- The IMD 1 layer comprises of an ~1.40 µm thick oxide.
- The vias and contacts comprise W and have a TiN liner. The vias partially penetrate into the top TiN liner of the metal layer below.



20220329 1544 11000 x_400282.png

Metal 2 and IMD 1 – TEM Cross-Section



General Structure_42_400973.png

Metal 2 and IMD 1 – SEM Cross-Section A-A

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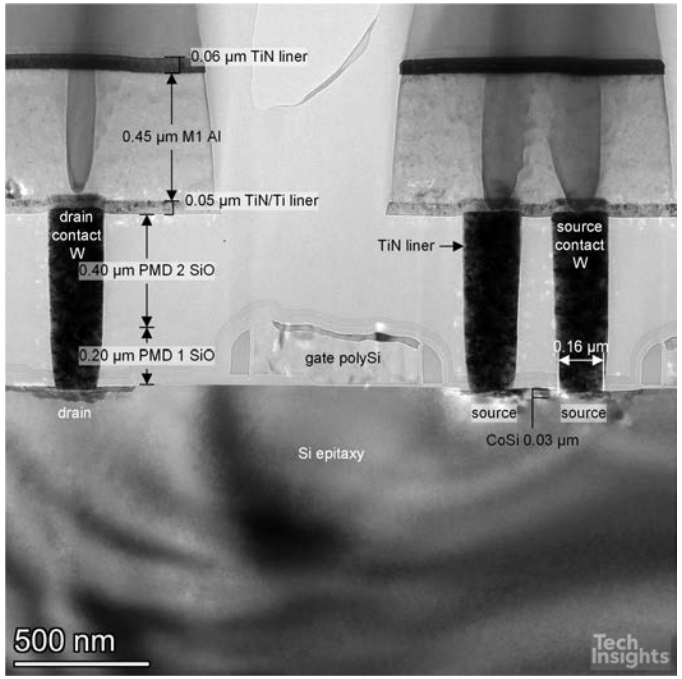
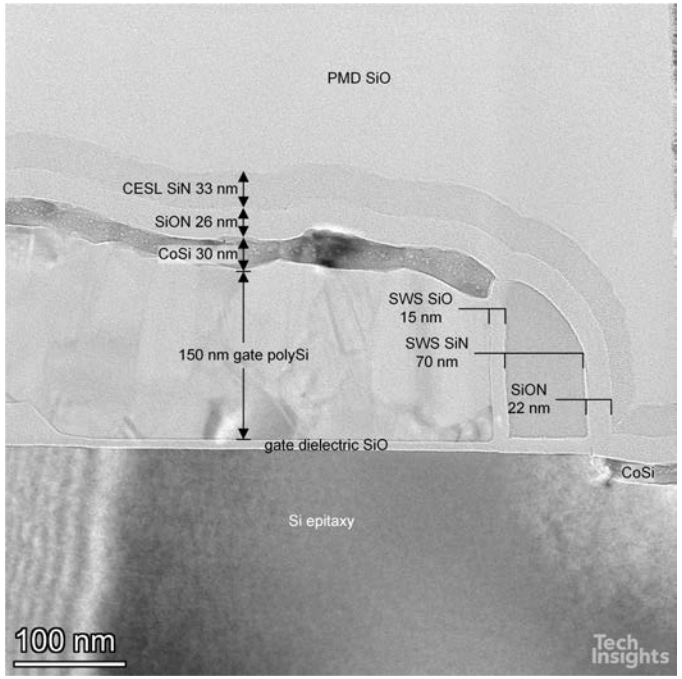
MP9502 Die Metal 1 and FEOL Structures

- Metal 1 comprises an ~0.06 µm thick top TiN liner, an ~0.45 µm thick Al layer, and bottom liners comprising ~0.05 µm thick TiN layers.
- The PMD comprises an ~0.4 µm thick oxide PMD 2 layer and an ~0.2 µm thick oxide PMD 1 layer.
- The S/D contact is ~0.16 µm wide at the bottom. The source, drain, and polysilicon contact regions use an ~30 nm thick CoSi layer.
- The gate polysilicon layer is ~180 nm thick, including ~30 nm thick CoSi layer.
- The sidewall spacer (SWS) comprises a 15 nm L-shaped SiO layer, a 70 nm D-shaped SiN layer.



20220329 1558 22500 x_400282.png

Metal 1 and PMD – TEM Cross-Section



20220329 1602 94000 × 0001_400282.png

HS/LS FET Gate SWS – TEM Cross-Section

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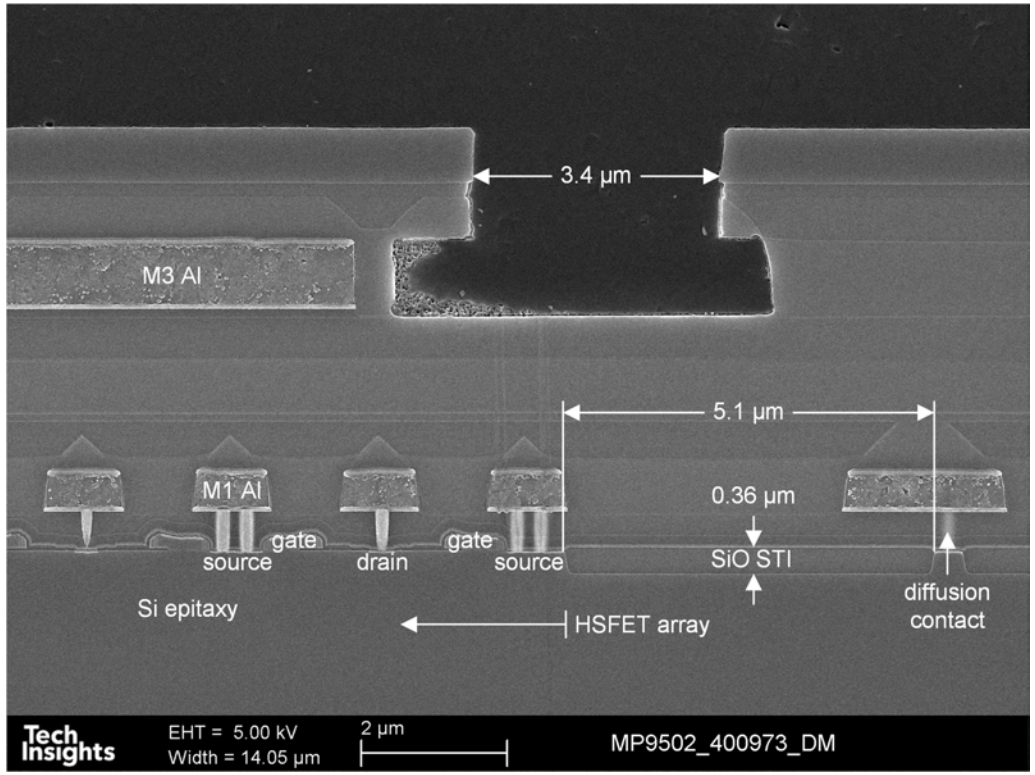
MP9502 Die Isolation Structures

- The MP9502 die employs SiO shallow trench isolation (STI) structures with ~0.36 µm depth as isolation between periphery circuit and HS/LS FET array.



General Structure_28_400973.png

STI – SEM Cross-Section A-A

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Periphery and Control Circuitry Device Analysis

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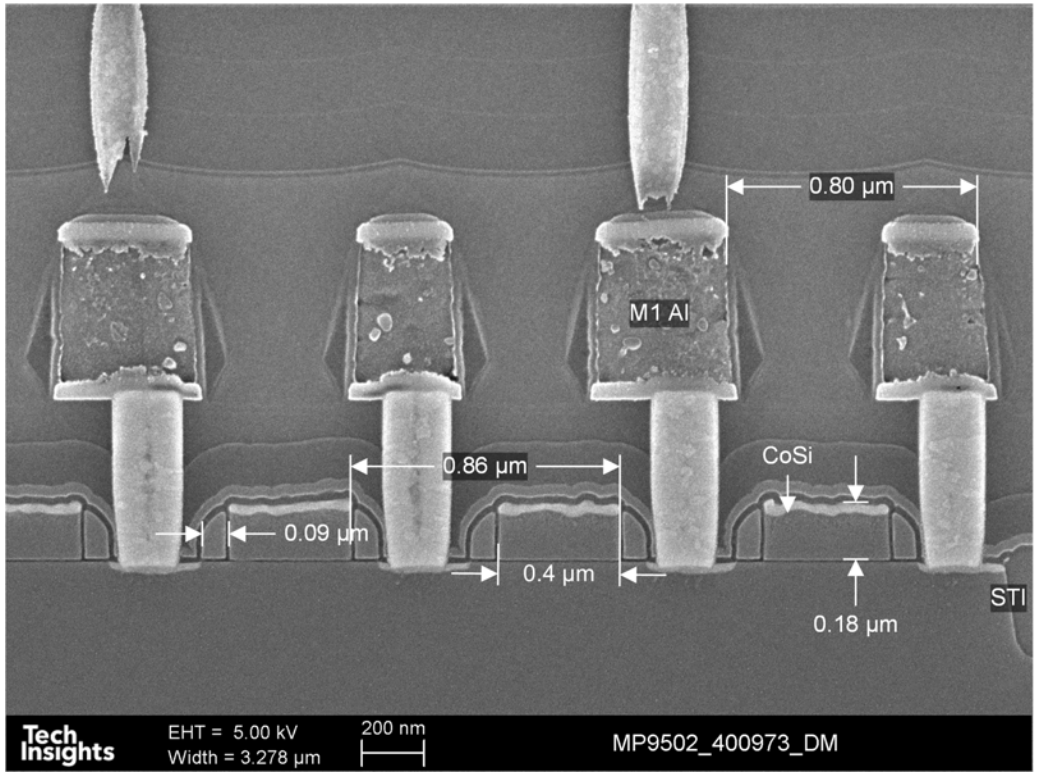
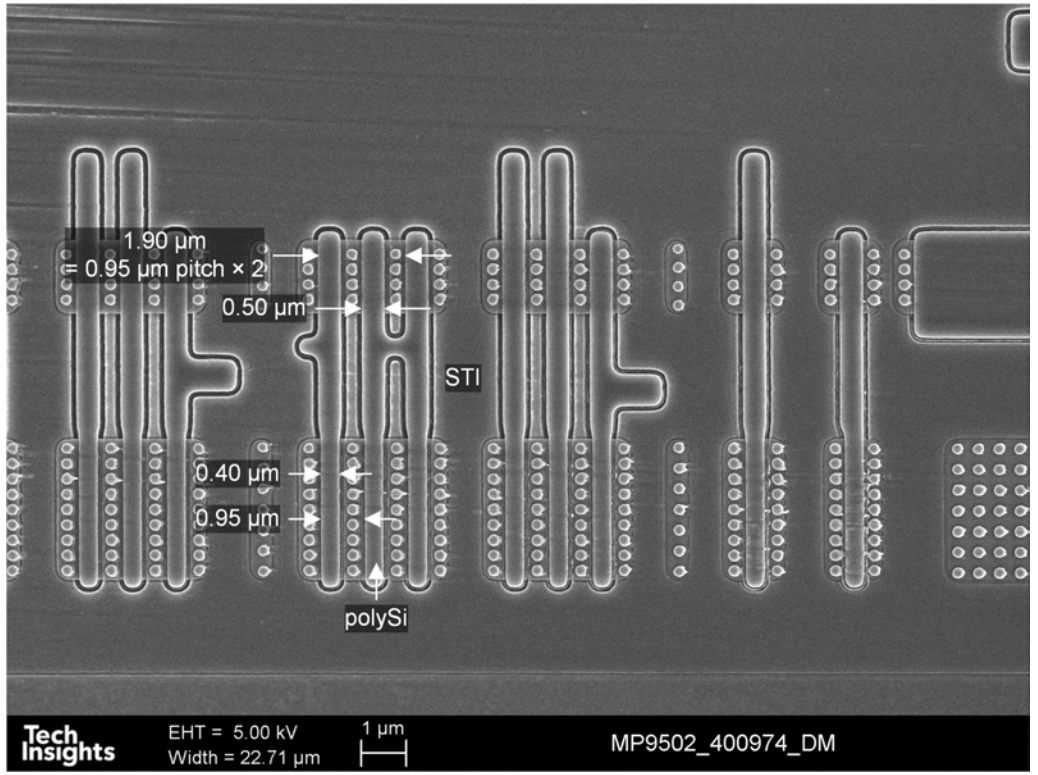
MP9502 Die Logic Transistors

- A minimum transistor gate length of 0.40 µm is observed in the logic transistors, the minimum observed contacted gate pitch is ~0.86 µm, and CoSi is used as gate silicide. These measurements are indicative of a likely relaxed 0.18 µm process.



Transistors_11_400973.png

Minimum Observed Gate Length and Contacted Gate Pitch – SEM Cross-Section A-A



Periphery_Poly_5K_44_400974.png

Minimum Observed Gate Length – SEM Plan View at the Gate Level

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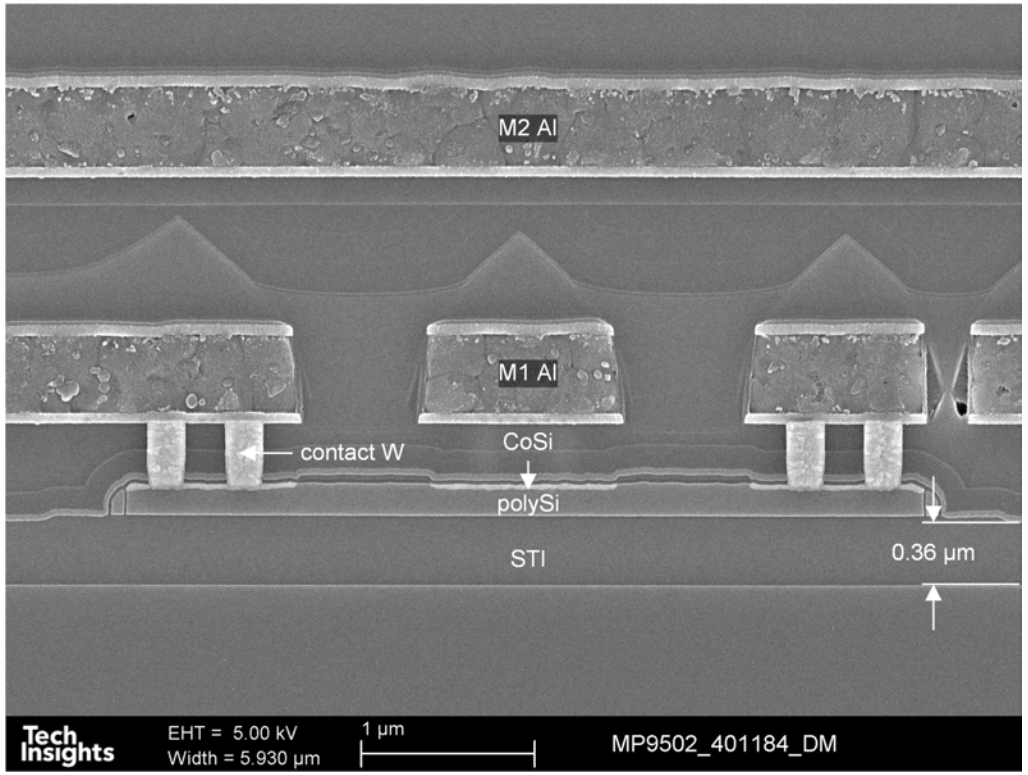
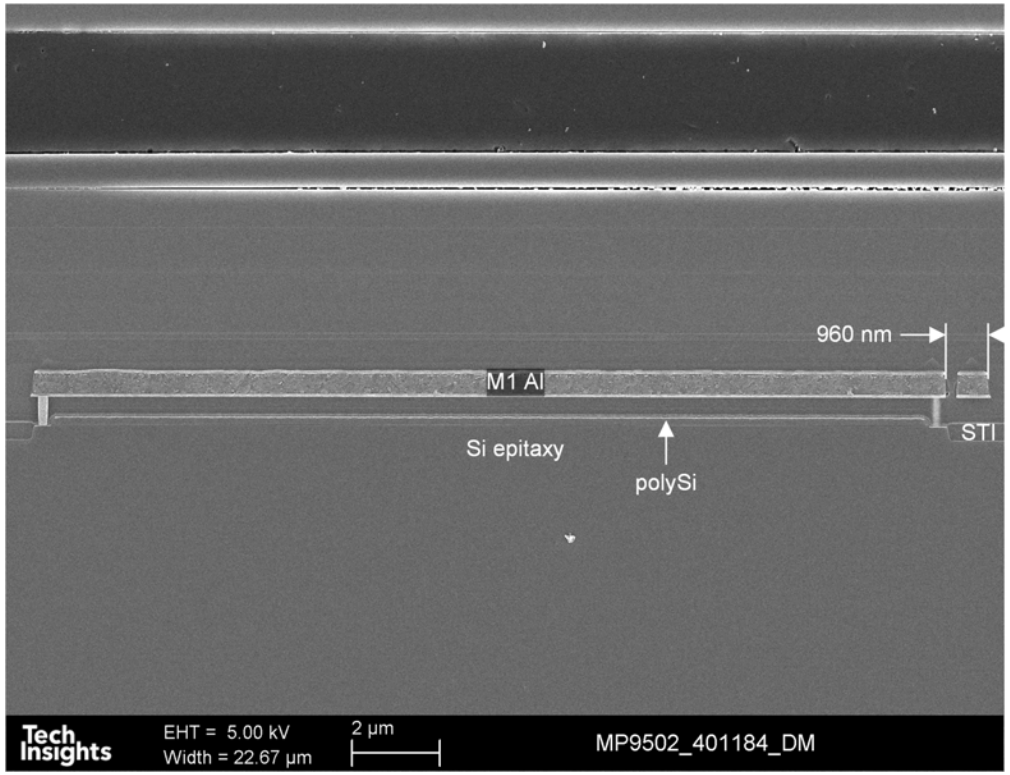
MP9502 Die Periphery Devices

- Observed periphery devices observed include BJTs (not analyzed), polysilicon resistors, and polysilicon MOS capacitors.
- Examples of polysilicon resistors and capacitors observed are shown below.



General Structure_20_401184.png

Polysilicon Resistors – SEM Cross-Section B-B



General Structure_26_401184.png

Polysilicon Capacitors – SEM Cross-Section B-B

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HS/LS FET Planar Analysis

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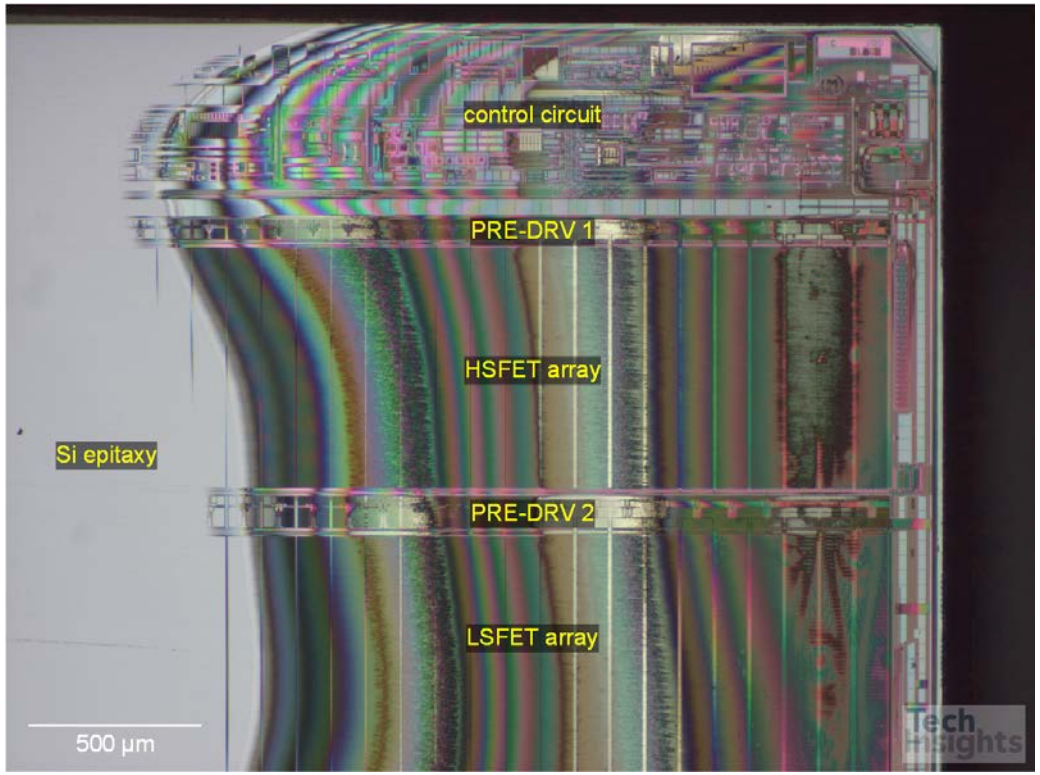
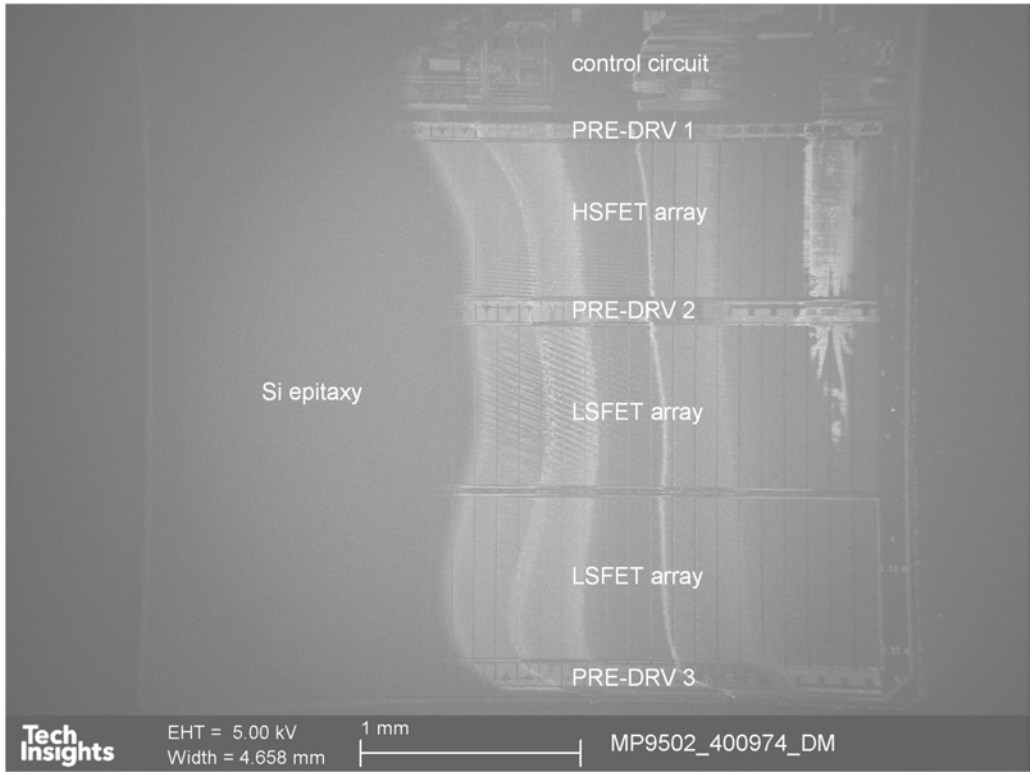
MP9502 Die HS/LS FET Array Overview

- One high side (HS) power MOSFET array and two low side (LS) power MOSFET arrays are arranged at the lower portion of the die.



Bevel Area_02_400974_5x1r.png

HS/LS FET Arrays – Optical Bevel



Bevel Section_01_400974.png

HS/LS FET Arrays – SEM Bevel

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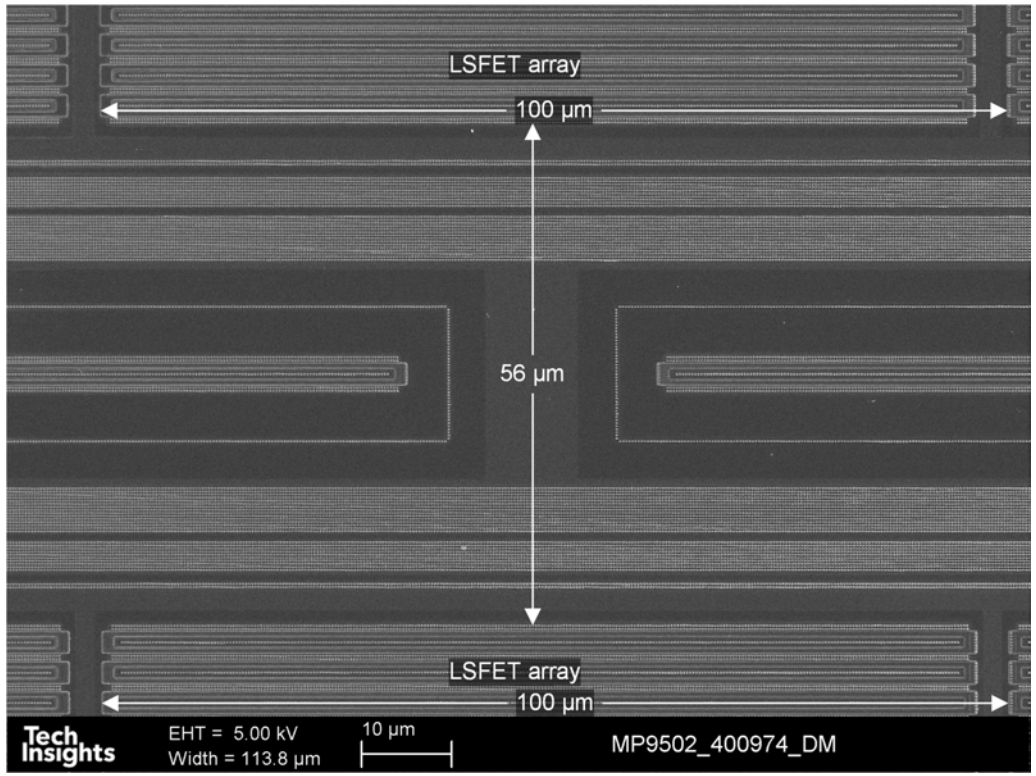
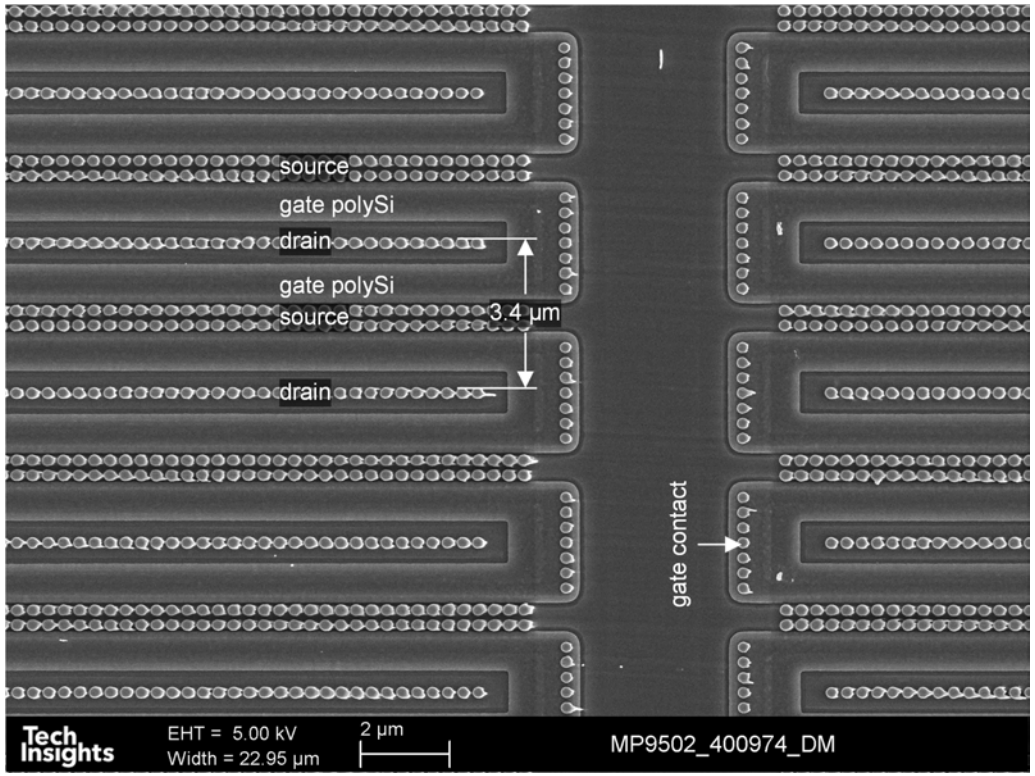
MP9502 Die LSFET Array

- The LSFET arrays measure ~100 µm pitch in the width direction, with a cell (drain-to-drain) pitch of ~3.4 µm in the LSFET array.
- Two groups of LSFET arrays are spaced ~56 µm apart vertically.



Gate Array_Interconnect_1K_26_400974.png

LSFET Array – SEM Plan View at the Gate Level



Gate Array_Poly_5K_08_400974.png

LS FET – SEM Plan View at the Gate Level

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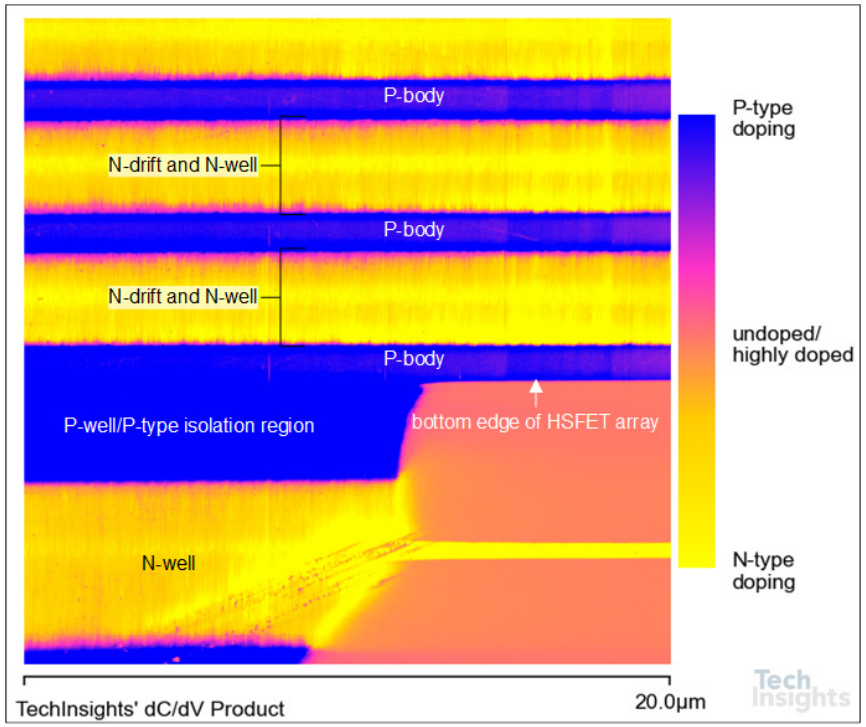
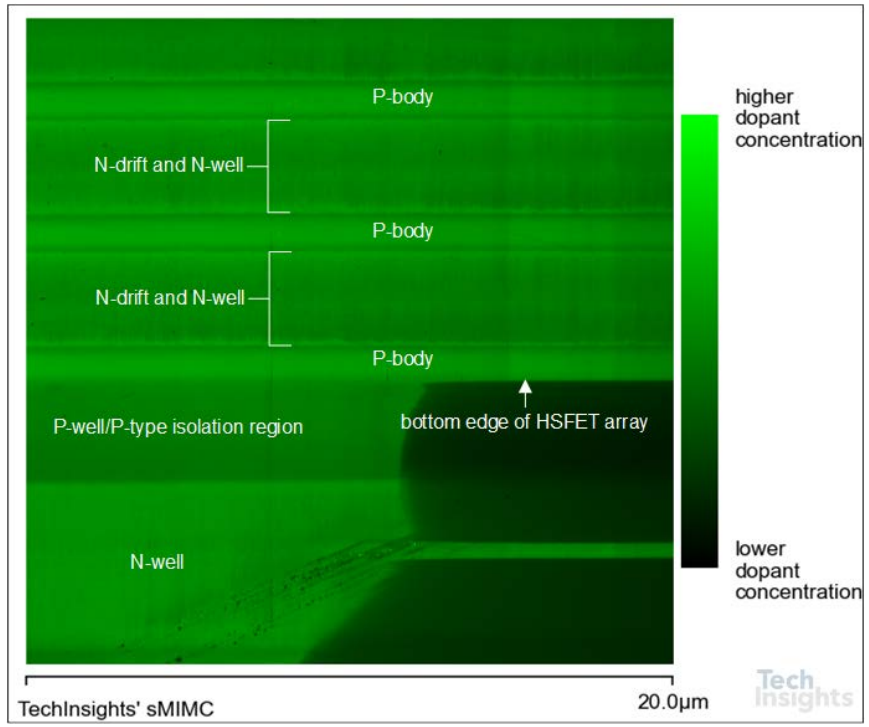
MP9502 Die HSFET Array Edge – P- and N-Type Regions

- Note: SCM imaging (left) is sensitive to dopant type, with N-type material giving a negative (yellow) response and P-type material giving a positive (blue) response. sMIM imaging (right) is sensitive to the dopant concentration level, with greater signal (brighter) corresponding to a higher dopant level, regardless of conductivity type.
- At the bottom edge of the HSFET array, a narrow N-well in the P-type isolation region is observed.



Array_edge_1to2_041122130327_PRODUCT_FRW_20.0u_512p_400974.png

Bottom Edge of the HSFET Array – SCM Bevel



Array_edge_1to2_041122130327_SMIMC_FRW_20.0u_512p_400974.png

Bottom Edge of the HSFET Array – sMIM-C Bevel

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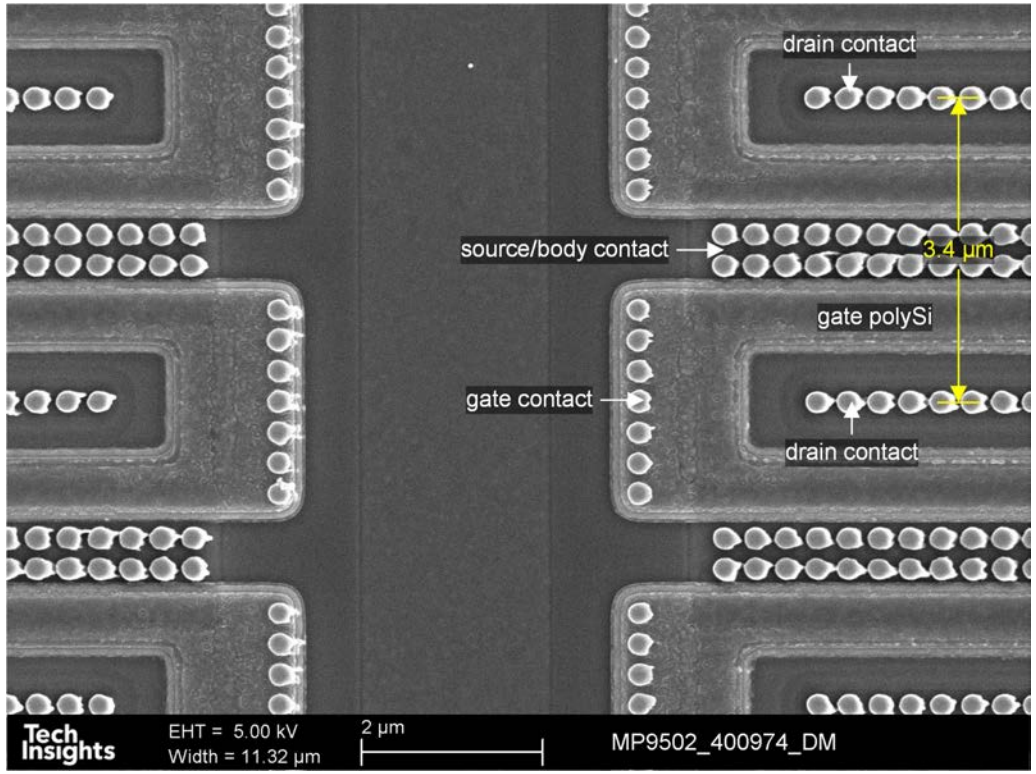
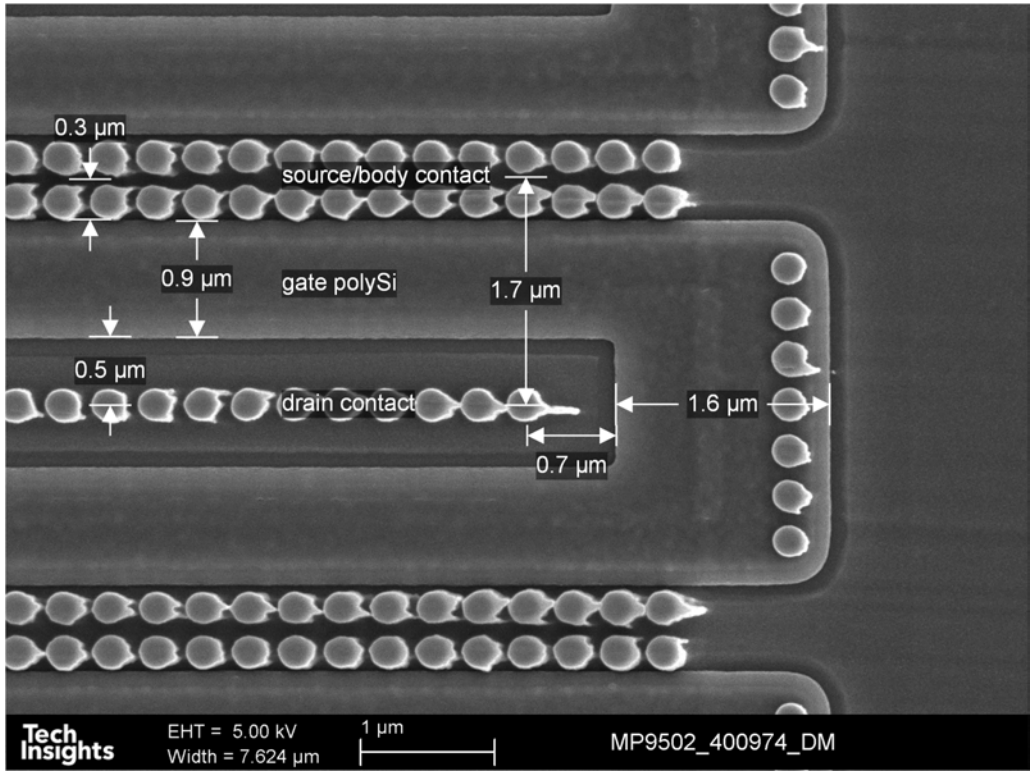
MP9502 Die LSFET Array – Polysilicon Level

- SEM bevel images below show the center region of the LSFET array at the polysilicon level.
- The cell (drain-to-drain) pitch measures ~3.4 µm, and the drain-to-source pitch measures ~1.7 µm in the LSFET array.



Gate Array_Poly_10K_47_400974.png

LSFET Array – SEM Bevel at the Gate Level



Gate Array_Poly_15K_09_400974.png

LSFET Array – SEM Bevel at the Gate Level

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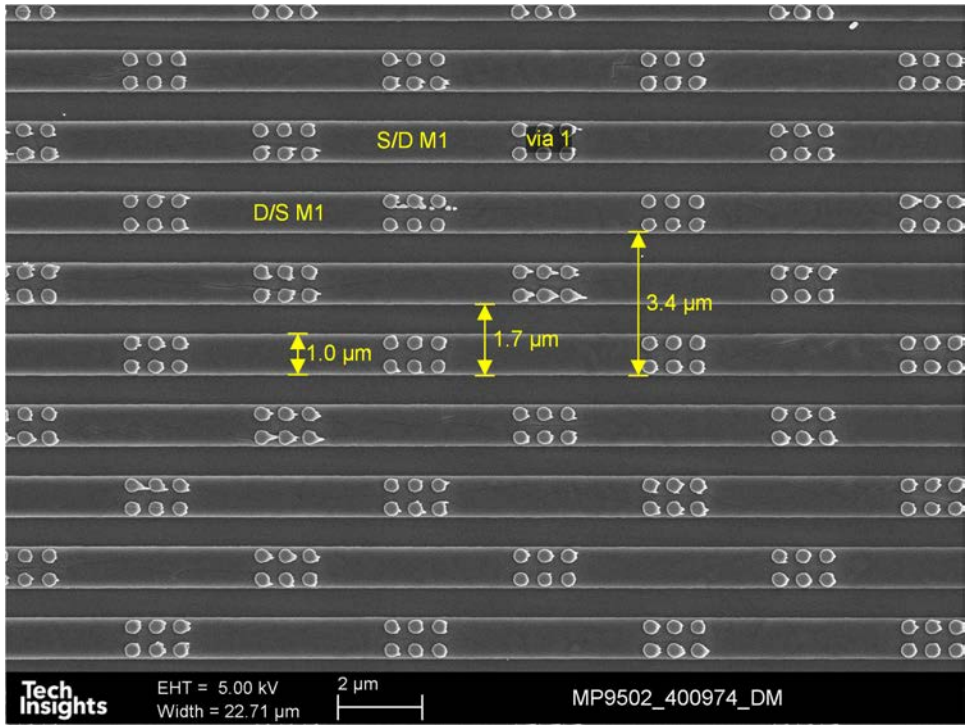
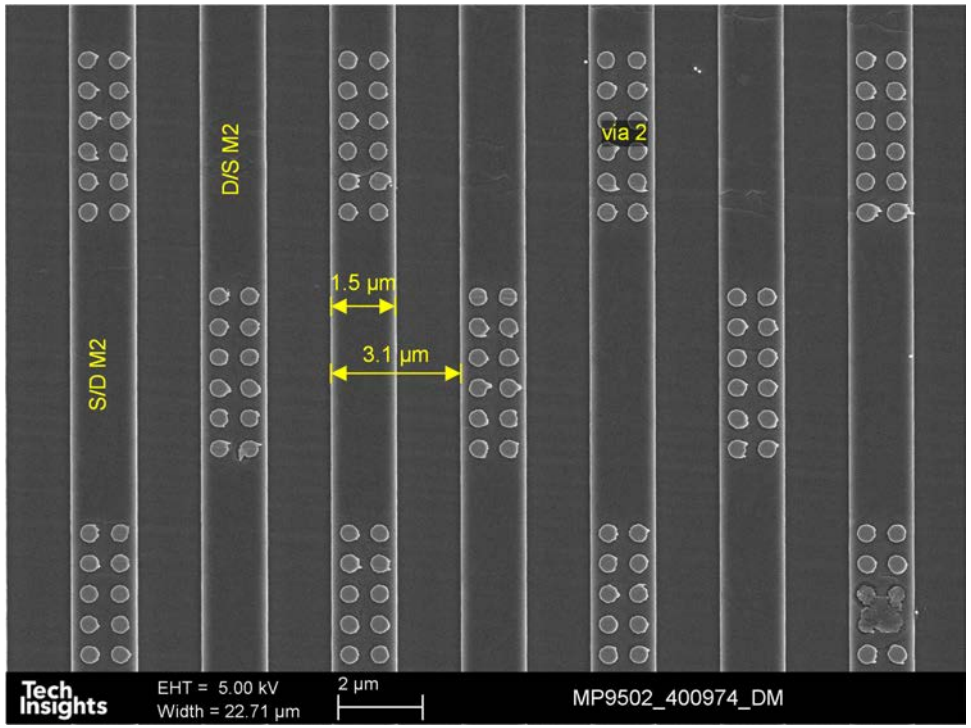
MP9502 Die LS FET Array – Metal 1 and Metal 2 Levels

- SEM bevel images below show the center region of the LSFET array at the metal 1 (M1) and metal 2 (M2) level.
- The M1 strips in the LSFET array area measure 1.0 µm with a 1.7 µm pitch, M2 strips measure 1.5 µm with a 3.1 µm pitch.
- The M1 and M2 strips are placed orthogonally with multiple rows and columns as the case of S/D vias 1 and 2.



Gate Array_M1_5K_13_400974.png

LSFET Array – SEM Bevel at the M1 Level



Gate Array_M2_5K_18_400974.png

LSFET Array – SEM Bevel at the M2 Level

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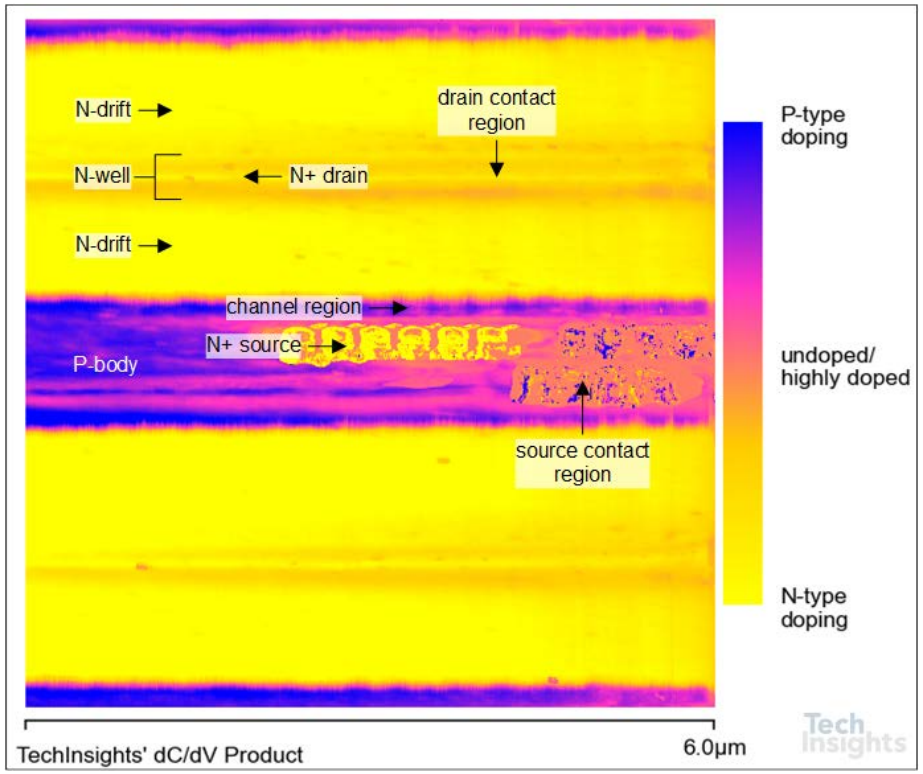
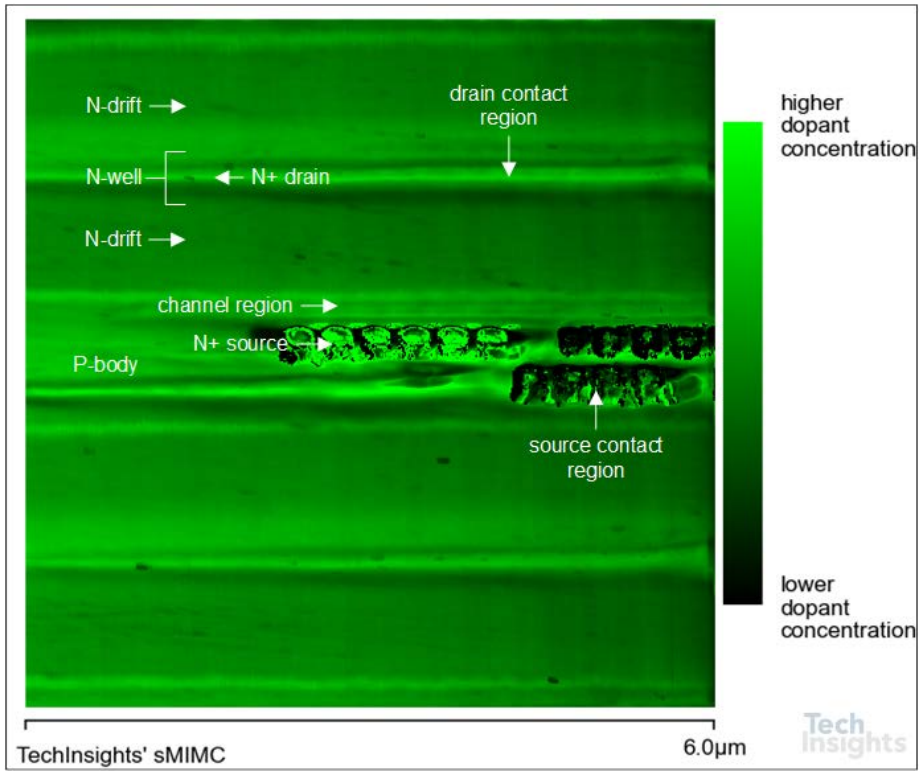
MP9502 Die LS FET Array – P- and N-Type Regions

- Strip doping regions can be seen along the length of the array. The N-type source region is only visible at the center-right side due to the bevel angle. It is more apparent in the cross-sectional analysis on page 38.



Array_below_poly_040822193718_PRODUCT_FRW_6.0u_512p_400974.png

LSFET Array – SCM Bevel



Array_below_poly_040822193718_SMIMC_FRW_6.0u_512p_400974.png

LSFET Array – sMIM-C Bevel

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HS/LS FET Cross-Sectional Analysis

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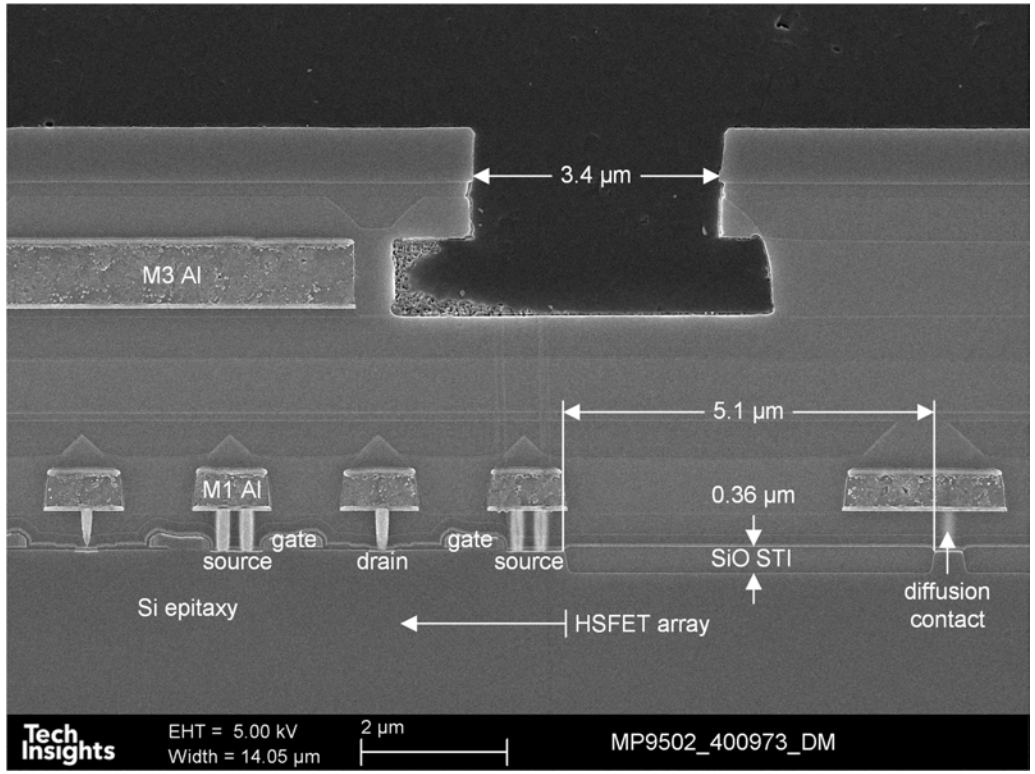
MP9502 Die HSFET Array Edge

- SEM cross-sections of the bottom edge of the HSFET array are shown. On the top side, a starting source contact is followed by a 5.1 µm wide STI.
- S/D passivation openings have a 3.4 µm wide window.



General Structure_28_400973.png

Top Edge of a HSFET Array – SEM Cross-Section A-A

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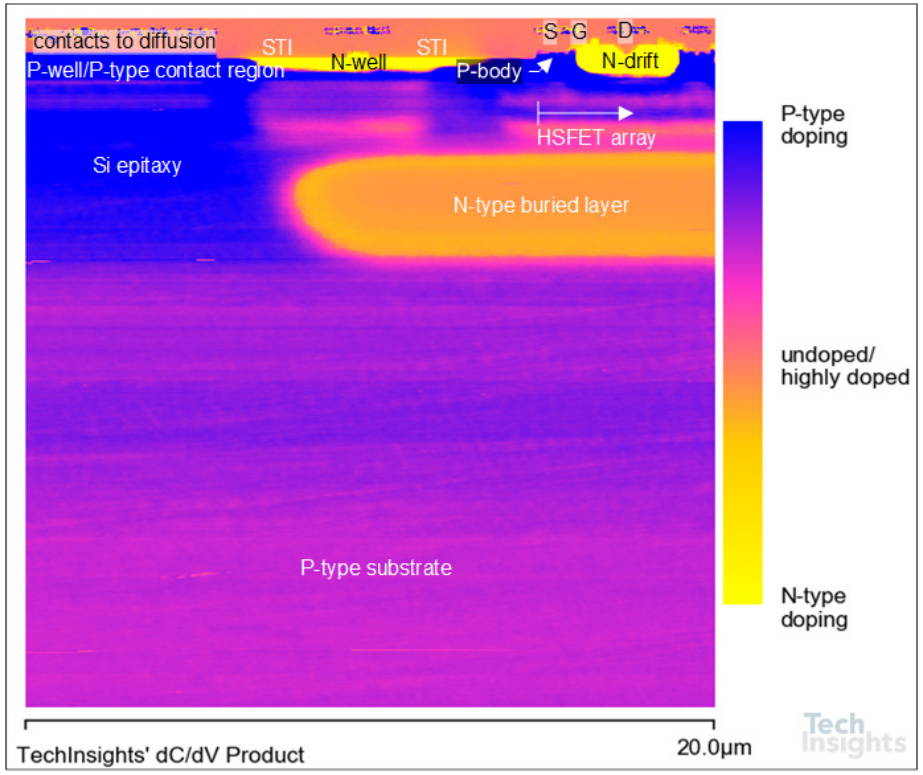
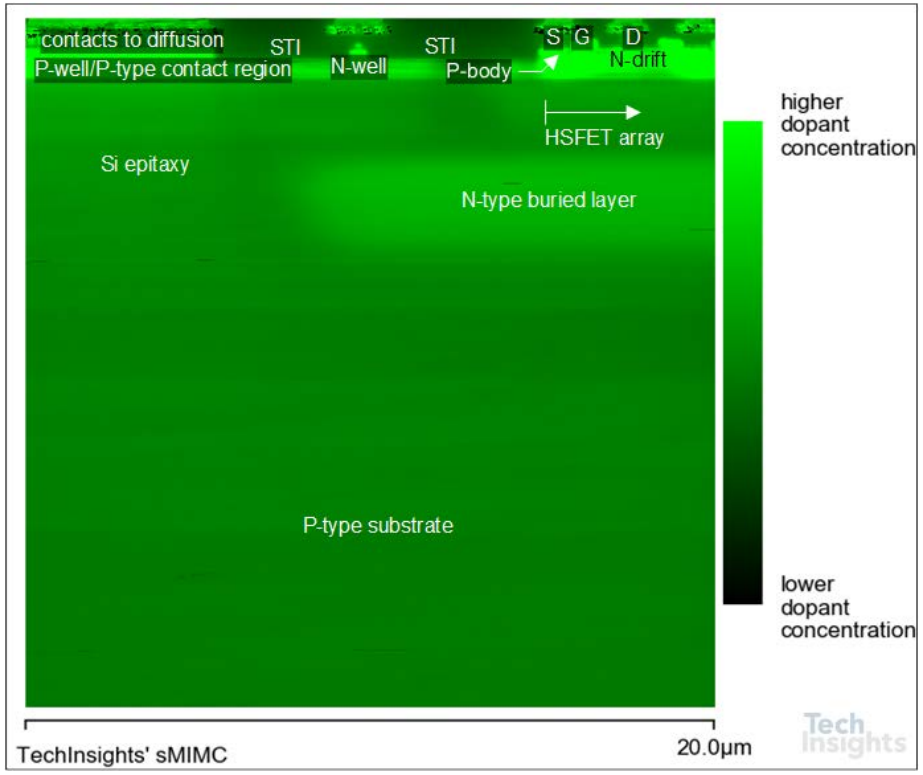
MP9502 Die HSFET Array Edge – P- and N-Type Regions

- SCM and sMIM-C analysis at the top edge region of HSFET array show the use of a P-type substrate, N-type buried layer (NBL), a P-well layer, likely epitaxial, and a P-well/P-type contact region between the output arrays.



Array_Edge_endarray1_040522190605_PRODUCT_FRW_20.0u_512p_400973.png

Edge of an HSFET Array – SCM Cross-Section A-A



Array_Edge_endarray1_040522190605_SMIMC_FRW_20.0u_512p_400973.png

Edge of an HSFET Array – sMIM-C Cross-Section A-A

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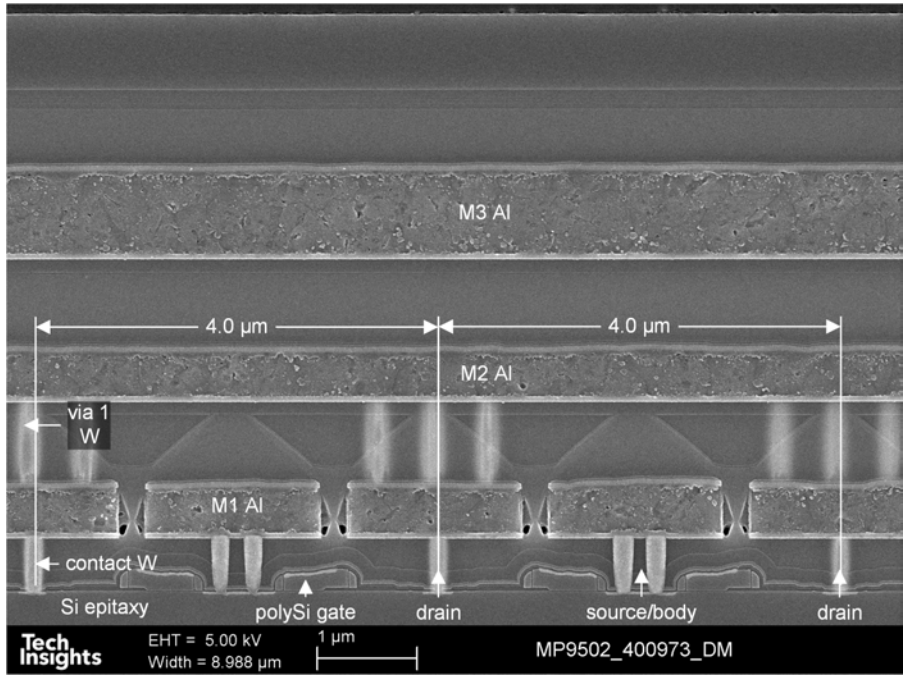
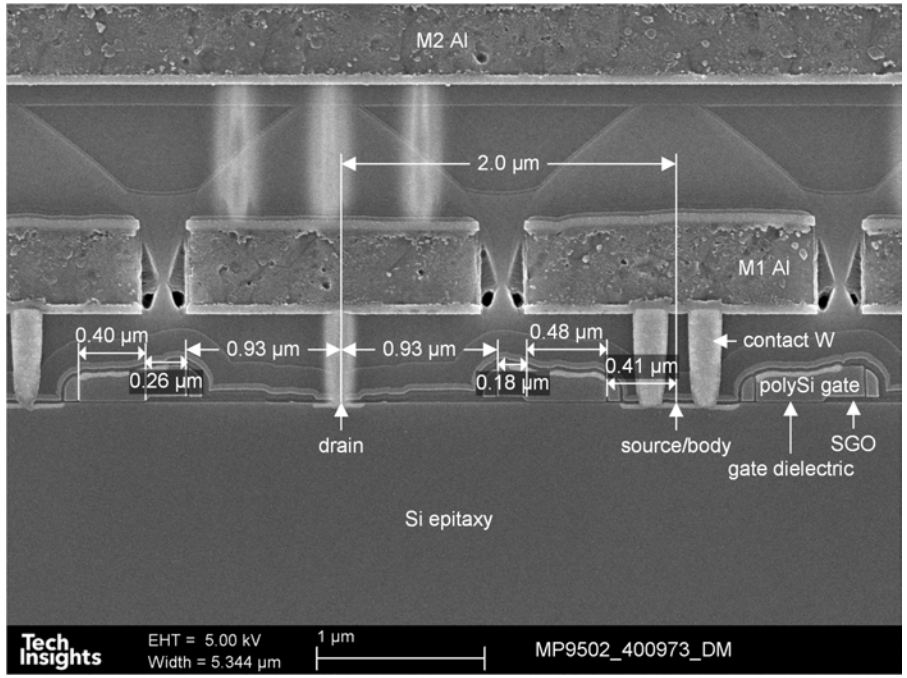
MP9502 Die HSFET Array

- The stepped-gate-oxide (SGO) are fabricated on this die. The use of SGO allows a reduction of on-resistance (Ron) compared with the conventional STI LDMOS [3].
- In the HSFET array, the cell (drain-to-drain) pitch measures ~4.0 µm, the gate to drain contact center spacing is ~0.93 µm, the gate to source/body contact center spacing is ~0.41 µm, the total polysilicon gate length is ~0.66 µm.
- In the HSFET array, there are two sets of polysilicon gate length combinations, one is ~0.40 µm physical channel length and ~0.26 µm extended portion over the SGO, another is ~0.48 µm physical channel length and ~0.18 µm extended portion over the SGO.



Transistors_18_400973.png

HSFET Array – SEM Cross-Section A-A



Transistors_19_400973.png

HSFET Array – SEM Cross-Section A-A

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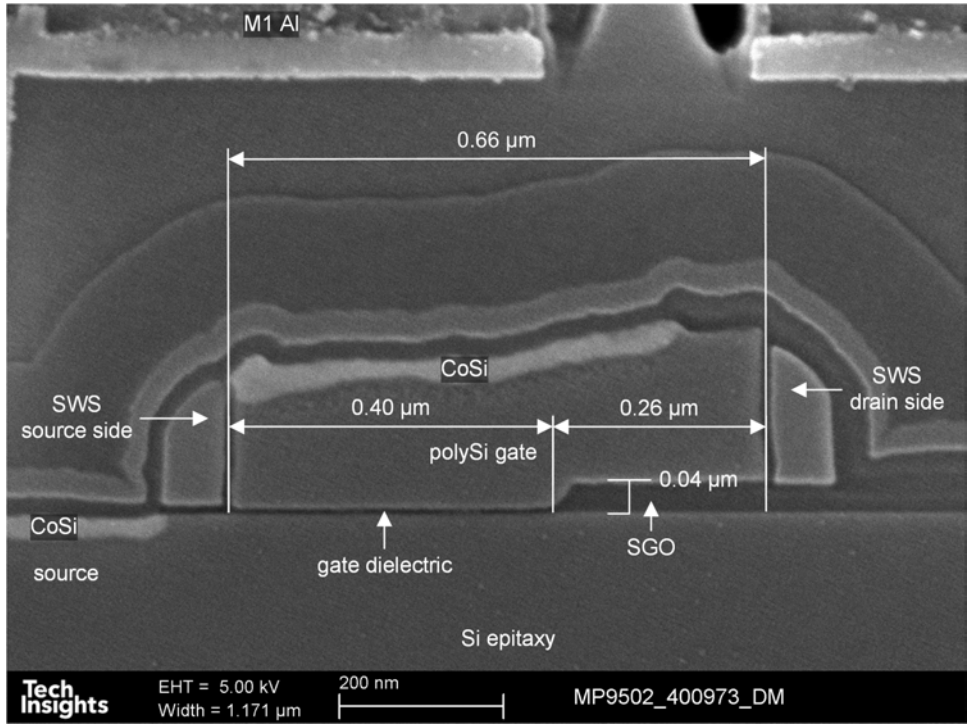
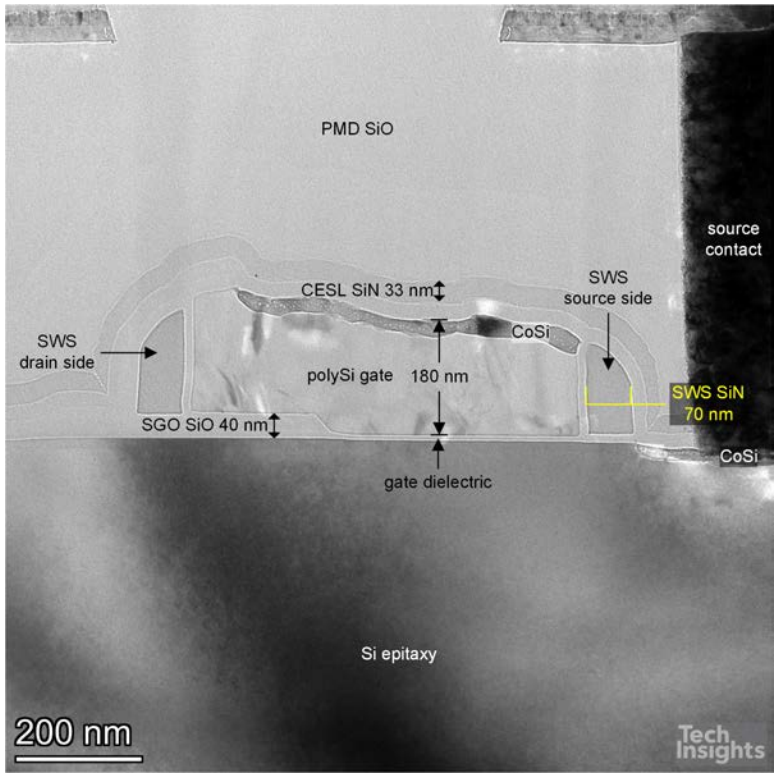
MP9502 Die HSFET Array

- In the HSFET array, the gate polysilicon strip measures ~0.66 µm, including the physical channel length of ~0.40 µm and the extended portion over the SGO in the analyzed region.
- The gate polysilicon is nominally ~180 nm thick, including the cobalt silicide (CoSi) layer.



Transistors_22_400973.png

HSFET Array – SEM Cross-Section A-A



20220329 1601 46000 x_400282.png

HSFET Array – TEM Cross-Section

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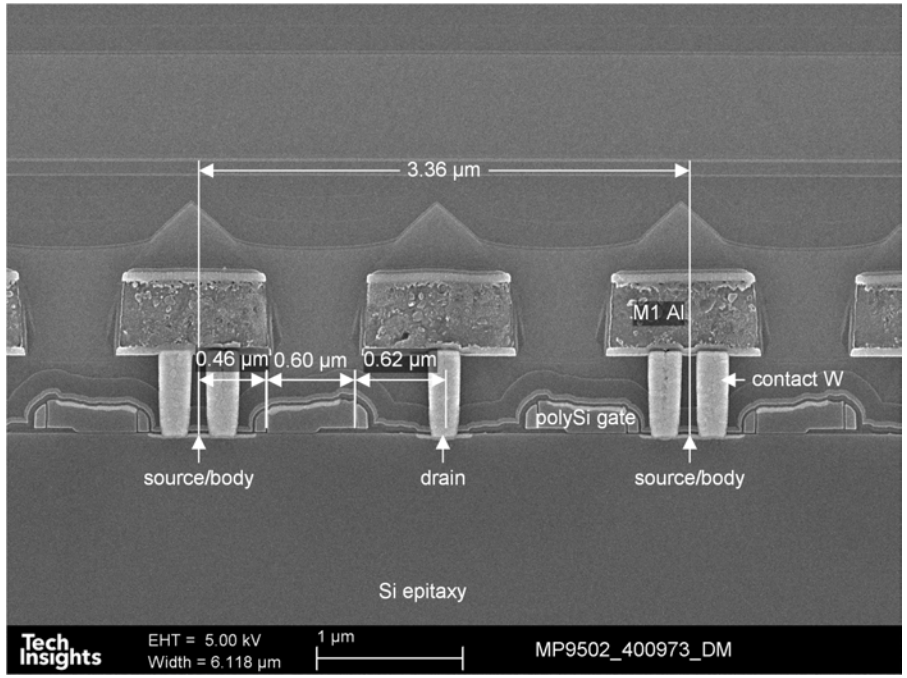
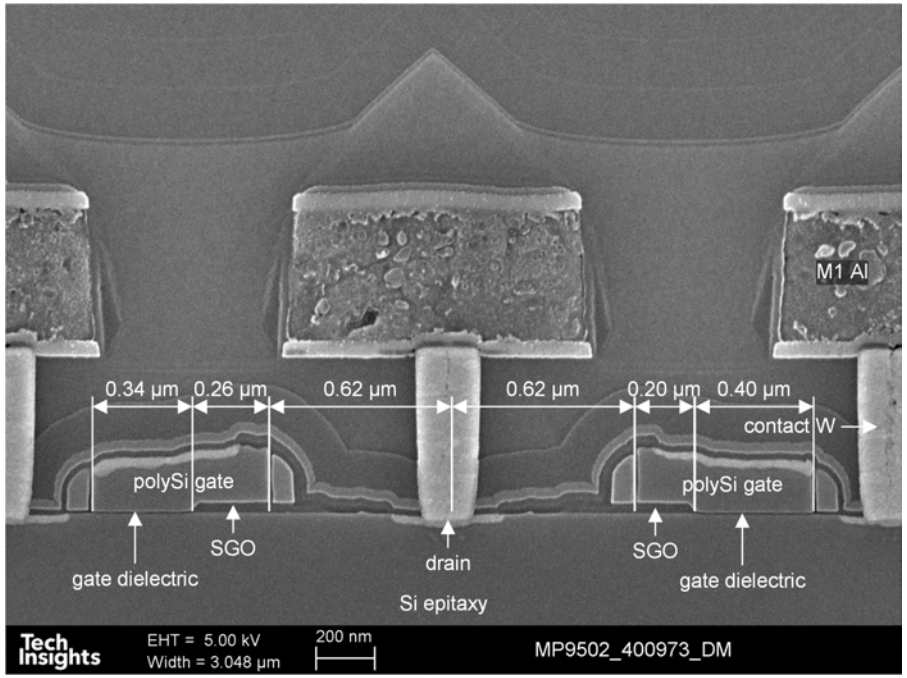
MP9502 Die LSFET Array

- The stepped-gate-oxide (SGO) are fabricated on this die. The use of SGO allows a reduction of on-resistance (Ron) compared with the conventional STI LDMOS [3].
- In the LSFET array, the cell (drain-to-drain) pitch measures ~3.36 µm, the gate to drain contact center spacing is ~0.62 µm, the gate to source/body contact center spacing is ~0.46 µm, the total polysilicon gate length is ~0.60 µm.
- In the LSFET array, there are two sets of polysilicon gate length combinations, one is ~0.34 µm physical channel length and ~0.26 µm extended portion over the SGO, another is ~0.40 µm physical channel length and ~0.20 µm extended portion over the SGO.



General Structure_47_400973.png

LSFET Array – SEM Cross-Section A-A



General Structure_48_400973.png

LSFET Array – SEM Cross-Section A-A

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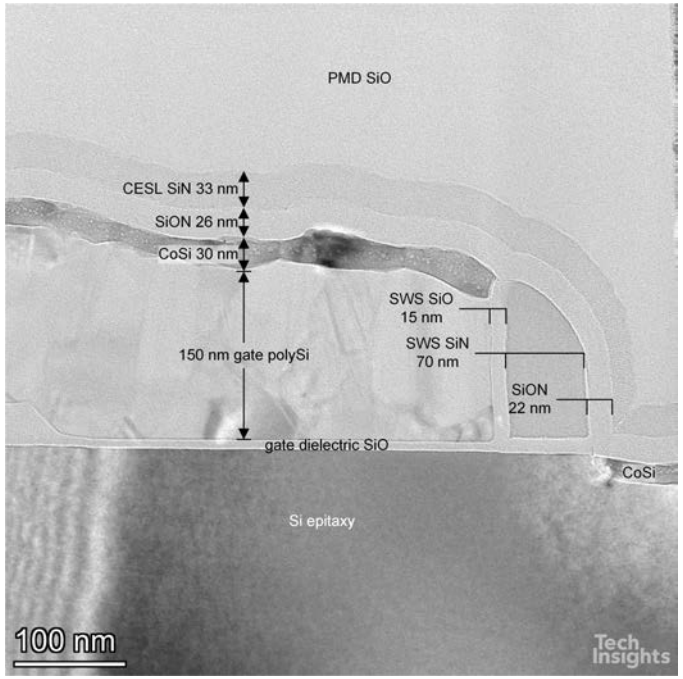
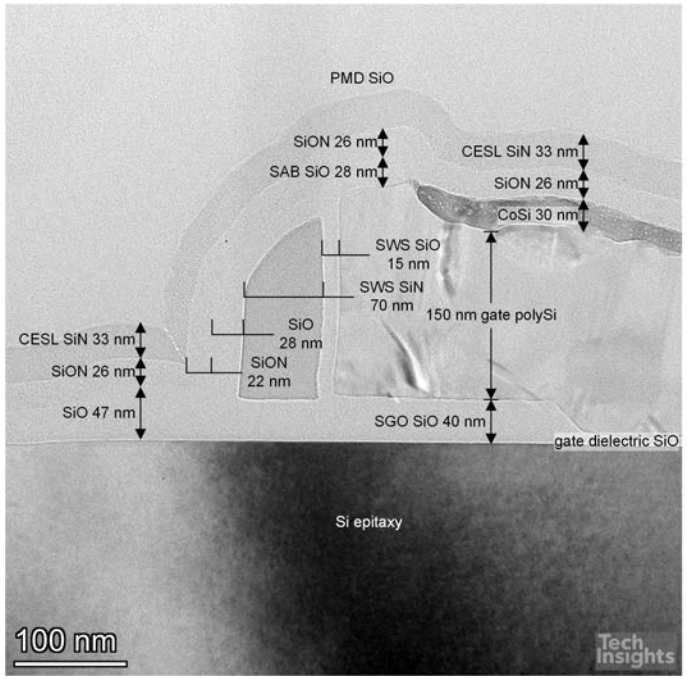
MP9502 Die HS/LS FET SWS

- The polysilicon contact regions use an, up to ~30 nm thick, CoSi layer.
- The sidewall spacer (SWS) comprises a 15 nm L-shaped SiO layer, a 70 nm D-shaped SiN layer, and a 22 nm D-shaped SiON on the S/D side.
- An additional 28 nm D-shaped SiO on the drain side only which is used as salicide block (SAB) layer. A 33 nm thick SiN CESL covers the transistors.
- The maximum thickness of oxide is ~47 nm in the region between polysilicon gate and drain contact.



20220329 1602 94000 × 0001_400282.png

HS/LS FET Gate SWS on Source Side – TEM Cross-Section



20220329 1601 94000 x_400282.png

HS/LS FET Gate SWS on Drain Side – TEM Cross-Section

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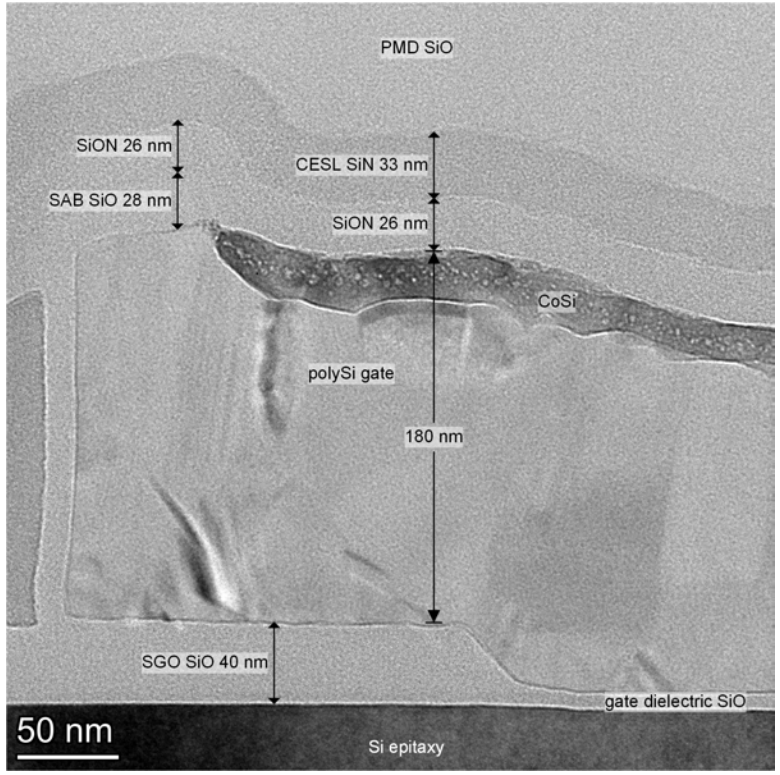
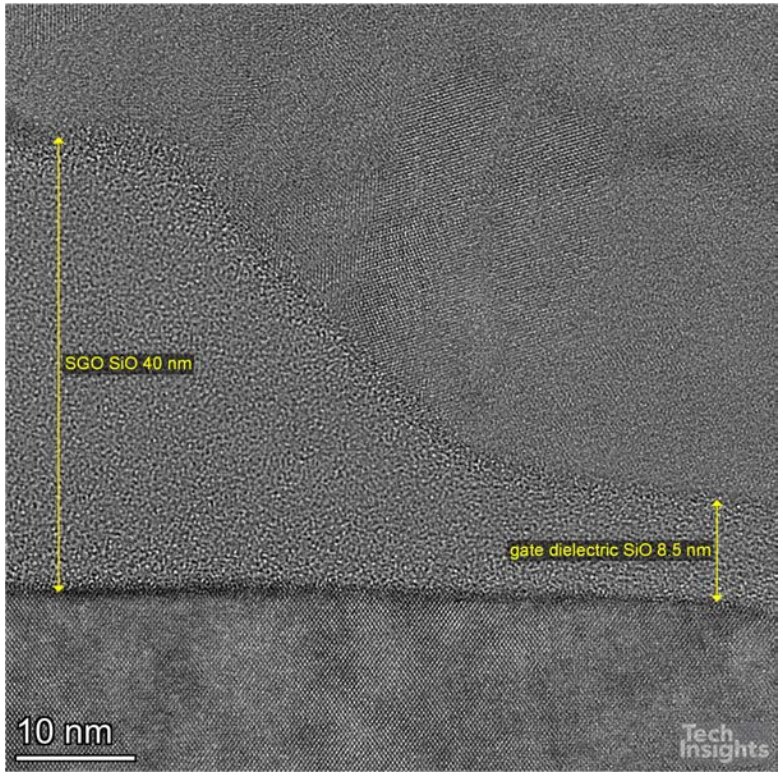
MP9502 Die HS/LS FET Gate Dielectric

- The gate features a ~40 nm thick SGO and an ~8.5 nm thick oxide as gate dielectric.



20220329 1605 150 kx 0001_400282.png

HS/LS FET Gate – TEM Cross-Section



20220329 1616 820 kx 0001_400282.png

HS/LS FET Gate Dielectric – TEM Cross-Section

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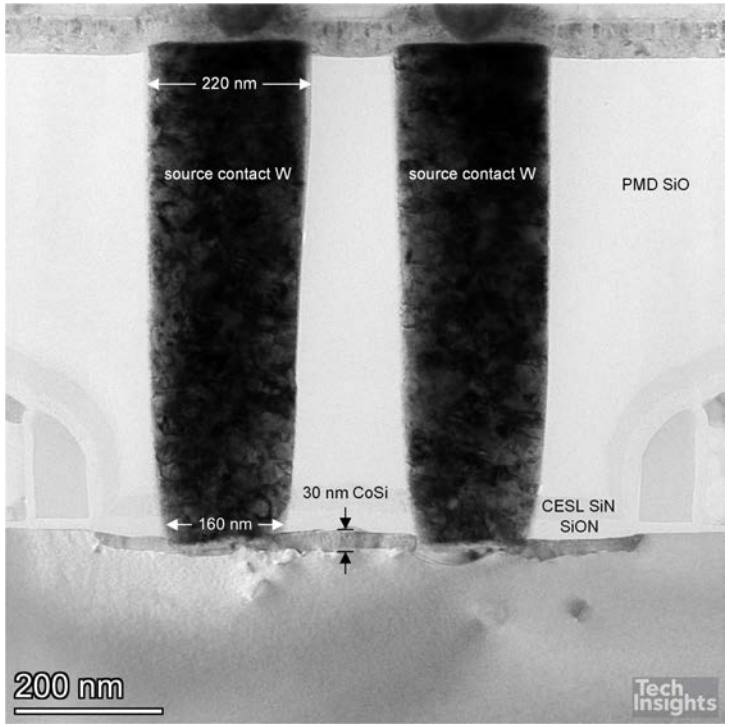
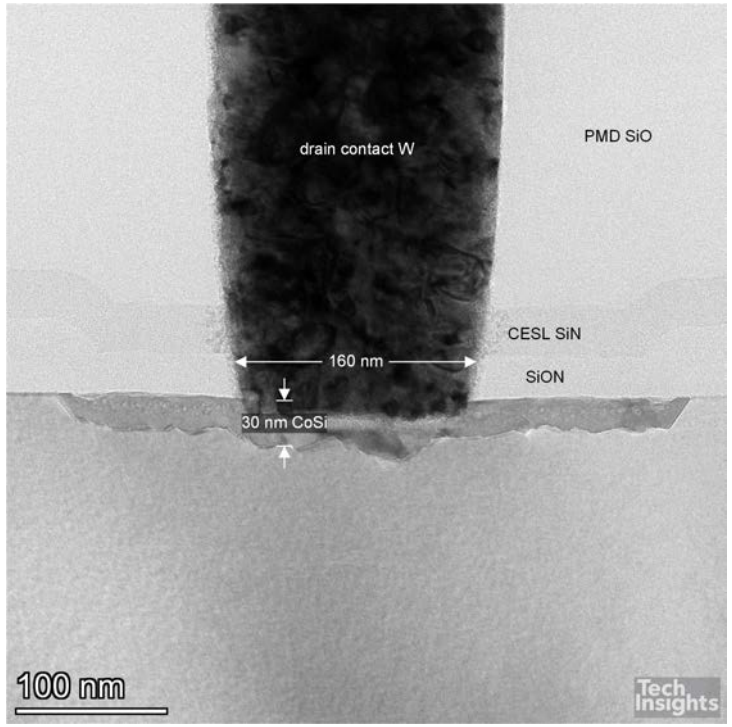
MP9502 Die HS/LS FET Contacts

- A CoSi region up to ~30 nm thick is observed in the source and drain contact regions.
- The S/D contact (W) partially penetrates into the top of the S/D ohmic contact layer (CoSi).
- The W contacts are ~0.22 µm in diameter at the widest portion and narrow down to 0.16 µm at the bottom.



20220329 1631 58000 x_400282.png

HS/LS FET Source Contacts – TEM Cross-Section



20220329 1555 120 kx_400282.png

HS/LS FET Drain Contact – TEM Cross-Section

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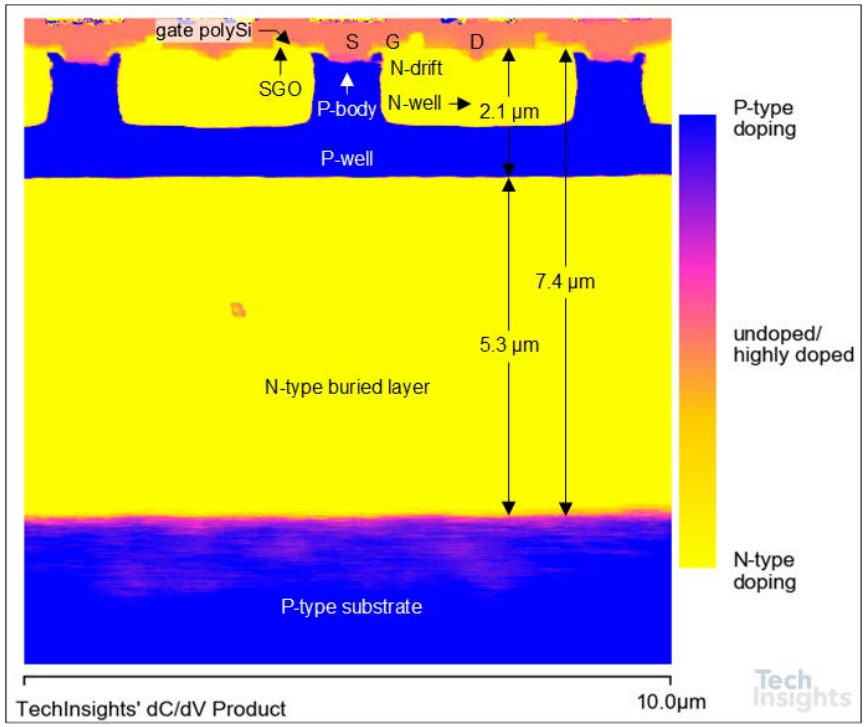
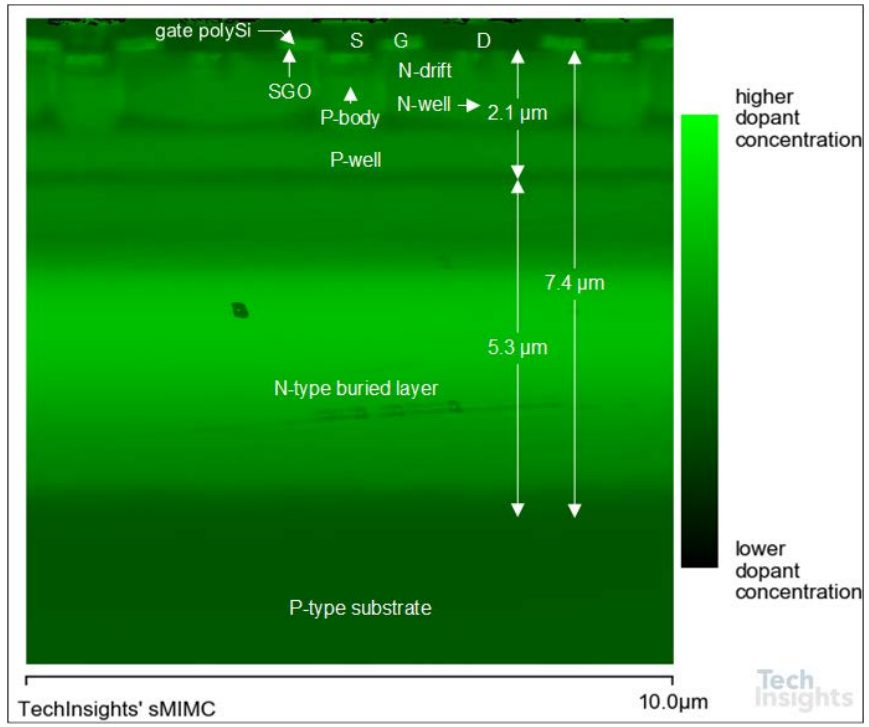
MP9502 Die HSFET Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the HSFET array show the use of a P-type body region, N-type drift region, and a higher-doped N-well at the drain region.
- The P-well layer starts ~2.1 µm from the front surface, while the NBL measures ~5.3 µm thick and reaches ~7.4 µm deep.
- NBL seems to have two regions of higher-doped lower portion and lower-doped upper portion in the Si body.



Array_040522164608_PRODUCT_FRW_10.0u_512p_400973.png

HSFET Array – SCM Cross-Section A-A



Array_040522164608_SMIMC_FRW_10.0u_512p_400973.png

HSFET Array – sMIM-C Cross-Section A-A

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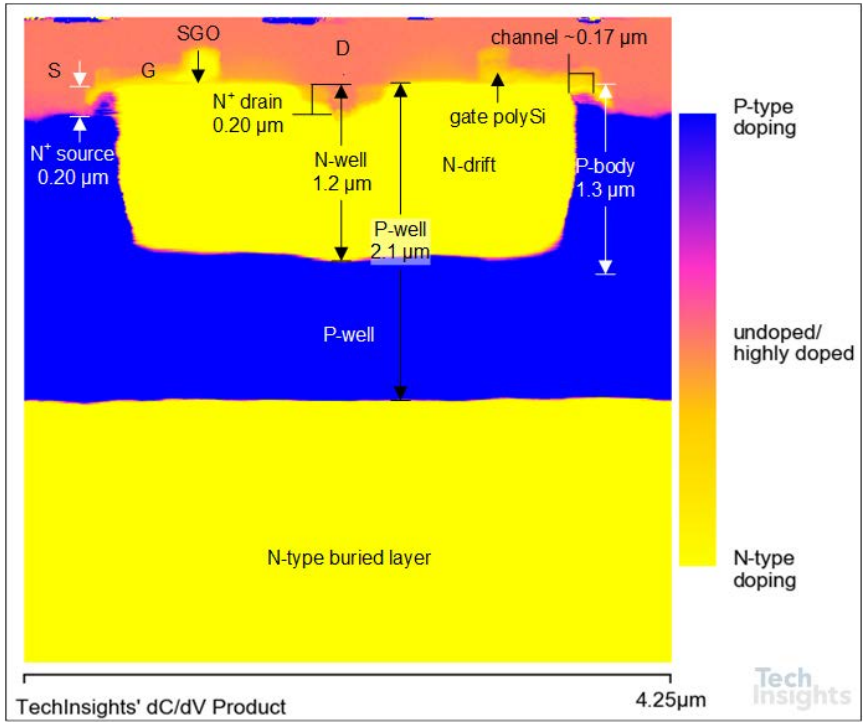
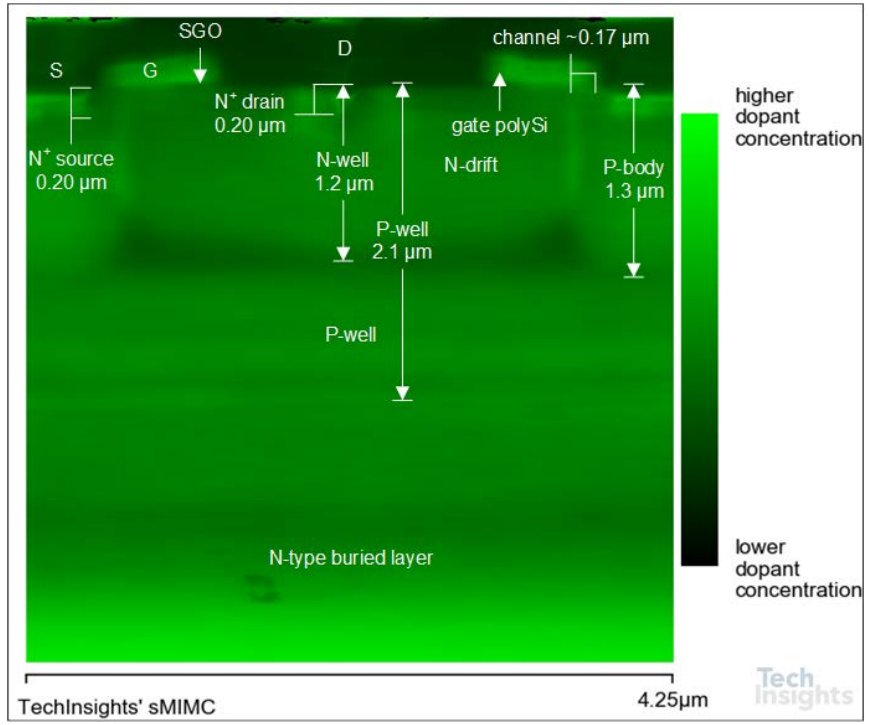
MP9502 Die HSFET – P- and N-Type Regions

- The N+ S/D regions are ~0.20 µm deep.
- The P-body is ~1.3 µm deep, while the drain N-well and N-drift region is ~1.2 µm deep.
- The effective channel length defined by dopant boundary is estimated to be ~0.17 µm.



Array_040522171710_PRODUCT_FRW_4.25u_512p_400973.png

HSFET – SCM Cross-Section A-A



Array_040522171710_SMIMC_FRW_4.25u_512p_400973.png

HSFET – sMIM-C Cross-Section A-A

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Comparison of 0.18 µm BCD Processes

- The MPS MP86905 analyzed in this report is compared with the following 0.18 µm BCD processes previous analyzed by TechInsights:

Feature	MPS MP86905	Maxim MAX77854 [4]	Texas Instrµments BQ24260YFF [5]	Qualcomm PM8921 [6]
Device type	PMIC	PMIC	Li-Ion PMIC	PMIC
Mode of operation	PWM	Undetermined	PWM	Undetermined
Rated voltage/current	4.5-18* V/50 A	Undetermined	4.2-28* V/2.5 A	Undetermined
Foundry	Undetermined	Maxim	Texas Instruments	TSMC
Die area (whole die)	3.38 mm × 3.14 mm	4.72 mm × 4.17 mm	2.40 mm × 2.40 mm	6.20 mm × 6.49 mm
Process generation/technology	0.18 µm BCD	0.18 µm BCD S18	0.18 µm LBC8 BCD	0.18 µm BCD
LDMOS cell (drain-to-drain) pitch	HSFET: 4.0 µm LSFET: 3.4 µm	P-LDMOS: 7.2 µm N-LDMOS: 5.0 µm	N-LDMOS Array 1: 4.7 µm N-LDMOS Array 2: 6.8 µm N-LDMOS Array 3: 3.5 µm	P-LDMOS Array 6: 4.3 µm N-LDMOS Array 7: 4.3 µm N-LDMOS Array 5: 9.3 µm
LDMOS gate dielectric thickness	8.5 nm	14 nm	13 nm	14 nm
LDMOS electrical channel length	~0.17 µm	P-LDMOS: 0.64 µm N-LDMOS: 0.68 µm	~0.30 µm	P-LDMOS Array 6: ~0.4 µm (assumed) N-LDMOS Array 7: ~0.8 µm (assumed) N-LDMOS Array 5: ~1.6 µm (assumed)
Isolation type(s)	STI	STI	STI	STI
Silicide	CoSi	CoSi	CoSi	CoSi
Number of metal layers and material	3 Al	4 Al	3 Al	5 Al
Contacts/vias material	W/W	W/W	W/W	W/W
Number of polysilicon layers	1	1	1	1

* The absolute maximum rating voltage

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[1] “Monolithic Power Systems,” Monolithic Power Systems website, https://www.monolithicpower.com/en/about-mps.html (accessed April 15, 2022)

[2] “MP86905 Intelli-Phase™ Solution with Integrated HS-/LS-FETs and Driver,” MPS datasheet, https://www.monolithicpower.com/en/documentview/productdocument/index/version/2/document_type/Datasheet/lang/en/sku/MP86905/ (accessed April 15, 2022)

[3] "Study on 20 V LDMOS With Stepped-Gate-Oxide Structure for PMIC Applications: Design, Fabrication, and Characterization,” S. -Y. Chen et al., IEEE Transactions on Electron Devices, Vol. 69, No. 2, pp. 878-881, Feb. 2022, doi: 10.1109/TED.2021.3131922.

[4] “Maxim MAX77854 PMIC 180 nm BCD S18 Process Review,” *Chipworks*, PPR-1605-801, August 5, 2016

[5] “Texas Instruments BQ24260YFF Li-Ion Power Management IC (TI LBC8 Process) Process Review,” *Chipworks*, PPR-1404-801, January 7, 2015

[6] “Qualcomm PM8921 PMIC (TSMC 180 nm BCD) Process Review,” *Chipworks*, PPR-1304-802, March 18, 2014

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Statement of Measurement Uncertainty and Scope Variation

Statement of Measurement Uncertainty

TechInsights calibrates length measurements on its scanning electron microscope (SEM), transmission electron microscope (TEM), and optical microscopes using measurement standards that are traceable to the International System of Units (SI).

Our SEM/TEM cross-calibration standard was calibrated at the National Physical Laboratory (NPL) in the UK (Report Reference LR0304/E06050342/SEM4/190). This standard has a 146 ± 2 nm (± 1.4%) pitch, as certified by the NPL. TechInsights verifies every six months that its SEM and TEM are calibrated to within ± 2% of this standard, over the full magnification ranges used.

TechInsights' optical microscopes are calibrated using a micrometer calibrated at the National Research Council of Canada (CNRC) (Report Reference LS-2005-0010). This standard has an expanded uncertainty of 0.3 µm (0.3%) for the micrometer's 100 µm pitch lines.

Random measurement errors, introduced during measurements of features on the calibrated images, yield an additional expanded uncertainty, which together with calibration uncertainty, is approximately ± 5% or better for features larger than about 20% of the image width.

TechInsights camera systems, used for package photographs and teardown photographs, and TechInsights X-ray instruments are not calibrated. Package dimensions are measured physically with calipers.

The materials analysis reported in TechInsights reports is normally limited to approximate elemental composition, rather than stoichiometry. Quantification of energy dispersive spectroscopy (SEM-EDS and TEM-EDS) and TEM-based electron energy loss spectroscopy (TEM-EELS) materials analysis usually not provided, unless otherwise stated. TechInsights will typically abbreviate the material composition, using only the elemental symbols (rather than full chemical formula) in approximate order of the peak heights in the spectra, but this does signify the relative concentration.

Secondary ion mass spectrometry (SIMS) data may be calibrated for certain dopant elements, provided suitable standards were available. Spreading resistance profiling (SRP) data is typically calibrated. Scanning microwave impedance microscopy (sMIM-C) provides spatial information on the dopant type; however, it is not quantitative. The accuracy of other methods is available on request.

Statement of Scope Variation

Due to the nature of reverse engineering and the diversity of analyzed devices, there is a possibility of content variation in TechInsights technical reports.

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TechInsights

1891 Robertson Road, Suite 500
Ottawa, Ontario K2H 5B7
Canada

T 1-613-599-6500
F 1-613-599-6501

Website: www.techinsights.com
Email: info@techinsights.com

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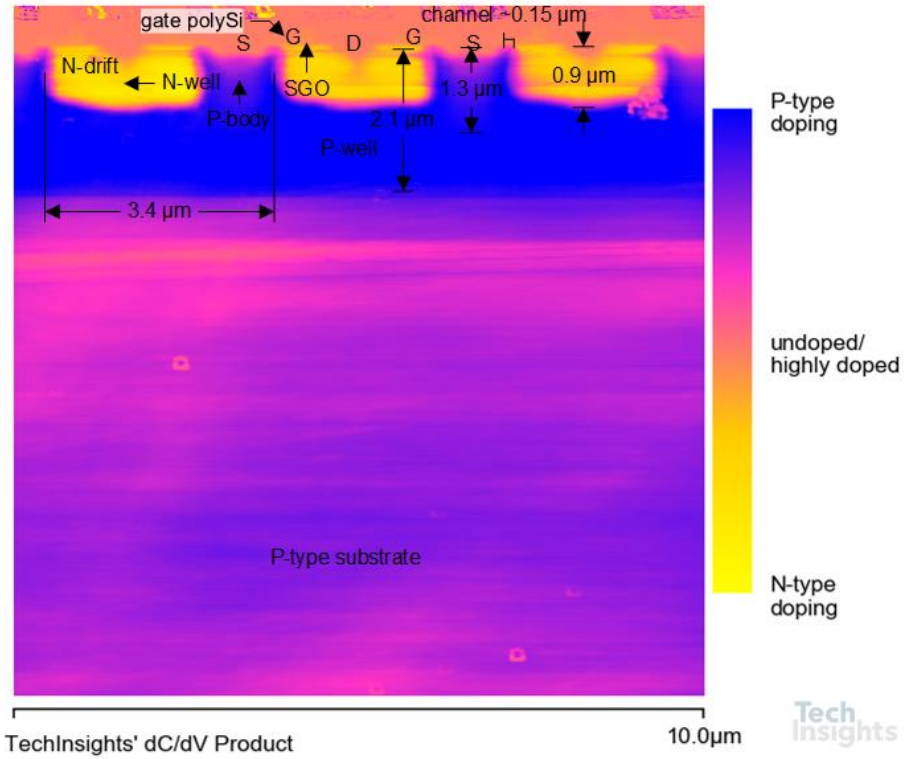
Supplemental Report for PEF-2202-801

(MPS MP86905 Monolithic Integrated HS/LS FETs and Driver PMIC Power Essentials)

Power Essentials Summary

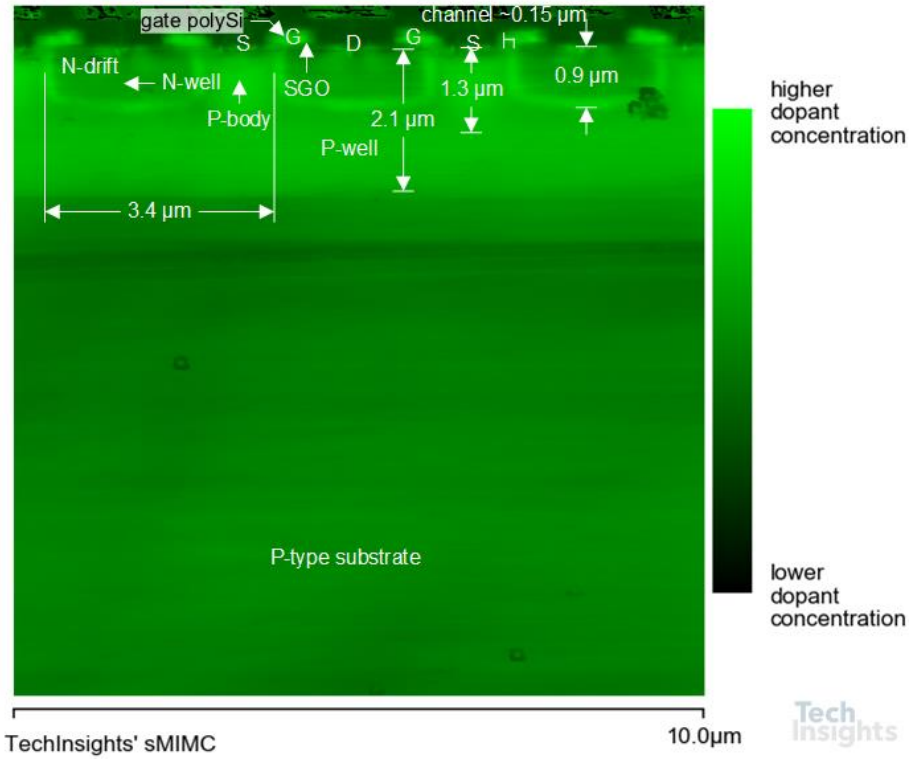
MP9502 Die LSFET Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the LSFET array show the use of a P-type body region, shallower N-drift/N-well in the drain region, and NBL is absent in the LSFET array.
- The P-well is ~2.1 µm deep, the P-body is ~1.3 µm deep, while the drain N-drift/N-well is ~0.9 µm deep, shallower than 1.2 µm observed in the HSFET array.
- Both HSFET and LSFET array likely share the P-well and P-body masks, but use different mask for drain drift region.
- The effective channel length defined by dopant boundary is estimated to be ~0.15 µm in the LSFET array.



Array_2_040622155352_PRODUCT_FRW_10.0u_512p_400973.png

LSFET Array – SCM Cross-Section A-A



Array_2_040622155352_SMIMC_FRW_10.0u_512p_400973.png

LSFET Array – sMIM-C Cross-Section A-A

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Statement of Measurement Uncertainty and Scope Variation

Statement of Measurement Uncertainty

TechInsights calibrates length measurements on its scanning electron microscope (SEM), transmission electron microscope (TEM), and optical microscopes using measurement standards that are traceable to the International System of Units (SI).

Our SEM/TEM cross-calibration standard was calibrated at the National Physical Laboratory (NPL) in the UK (Report Reference LR0304/E06050342/SEM4/190). This standard has a 146 ± 2 nm (± 1.4%) pitch, as certified by the NPL. TechInsights verifies every six months that its SEM and TEM are calibrated to within ± 2% of this standard, over the full magnification ranges used.

TechInsights' optical microscopes are calibrated using a micrometer calibrated at the National Research Council of Canada (CNRC) (Report Reference LS-2005-0010). This standard has an expanded uncertainty of 0.3 µm (0.3%) for the micrometer's 100 µm pitch lines.

Random measurement errors, introduced during measurements of features on the calibrated images, yield an additional expanded uncertainty, which together with calibration uncertainty, is approximately ± 5% or better for features larger than about 20% of the image width.

TechInsights camera systems, used for package photographs and teardown photographs, and TechInsights X-ray instruments are not calibrated. Package dimensions are measured physically with calipers.

The materials analysis reported in TechInsights reports is normally limited to approximate elemental composition, rather than stoichiometry. Quantification of energy dispersive spectroscopy (SEM-EDS and TEM-EDS) and TEM-based electron energy loss spectroscopy (TEM-EELS) materials analysis usually not provided, unless otherwise stated. TechInsights will typically abbreviate the material composition, using only the elemental symbols (rather than full chemical formula) in approximate order of the peak heights in the spectra, but this does signify the relative concentration.

Secondary ion mass spectrometry (SIMS) data may be calibrated for certain dopant elements, provided suitable standards were available. Spreading resistance profiling (SRP) data is typically calibrated. Scanning microwave impedance microscopy (sMIM-C) provides spatial information on the dopant type; however, it is not quantitative. The accuracy of other methods is available on request.

Statement of Scope Variation

Due to the nature of reverse engineering and the diversity of analyzed devices, there is a possibility of content variation in TechInsights technical reports.

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TechInsights

1891 Robertson Road, Suite 500
Ottawa, Ontario K2H 5B7
Canada

T 1-613-599-6500
F 1-613-599-6501

Website: www.techinsights.com
Email: info@techinsights.com

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